Abstract

In this project, six grid synchronisation techniques' performance have been tested under thirteen voltage faults tests.

In order to achieve synchrony with a three-phase voltage input, a PLL or Phase-Locked Loop is used. This control System processes the input signal and detects its phase by means of a series of mathematical transformations and filtering techniques that are detailed in this project.

Phase-Locked Loops are an essential part of any synchronous control system. The phase output of the PLL is used to ensure the stable performance of grid-connected equipment, especially in the case of power converters used in grid power injection from renewable sources.

Under balanced conditions PLL performance is very consistent. However, under disturbances in the voltage input the performance of many PLLs is compromised. Thirteen tests that include the most common kinds of faults have been designed in order to test the performance of the six studied PLL designs. All of the simulations have been carried out with Matlab SIMULINK software.

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Glossary

Acronyms

AC	Alternating current
PLL	Phase-Locked Loop
SRF	Synchronous Reference Frame
SOGI	Second Order Generalised Integrator
DDSRF	Double Decoupling Synchronous Reference Frame
AB	Alfa Beta
THD	Total Harmonic Distortion
LPF	Low Pass Filter
CITCEA	Centre d'Innovació Tecnològica en Convertidors Estàtics i Accionaments
DC	Decoupling

Preface

Contextualisation

The increase in demand of versatile and transportable energy has been blatant since the beginning of the 21st century. Mankind has been getting used to high energy demand commodities and the need for efficient energy generation and distribution systems is higher than ever. Research in this field is essential for the development of sustainable solutions to this ever-growing demand.

With social awareness about the consequences of fossil fuel dependence on the rise and blatant manifestations of climate change, the renewable energy sector has grown considerably in the latter years. The energy generated by these means must be injected into the grid efficiently in order to improve the competitiveness of wind and solar power.

The way in which the grid is powered by sources of very different nature emphasises the need for systems that manage them effectively. This is research and development of power converters becomes imperative.

Groups like the CITCEA in the UPC study and develop control systems for various kinds of converters, providing flexibility and optimising performance.

Motivation

Upon nearing the end of my degree, the need to learn about new fields of engineering pushed me on to search for an internship in research. The general approach of the degree provided an insight to many different subjects, but a lack of in depth study of any of them. Since my arrival at the CITCEA, the approach has been much more stimulating. Applying system dynamics analysis and mathematical transformations to the world of electric engineering has expanded my knowledge greatly on the subject. Upon studying this area in depth, I have acquired the motivation to pursue the electrical engineering specialisation in the industrial engineering master's degree.

Upon arrival at the CITCEA lab, the Matlab simulation of a voltage source converter (VSC) posed a great challenge that introduced me to the control of an electrical system. The control system of the VSC consisted in a Phase-Locked Loop, a current control loop and a DC control Loop. The Phase-Locked loop that was implemented in the simulation was very simplistic, and most of the members of the lab used the same design. Upon discussing this topic with the tutor, the study of new designs of PLLs and their performance under certain situations became a very interesting subject. The motivation behind this project lies both in producing a piece of work that will serve as a repository of ready-to-use PLL blocks in SIMULINK, and to understand the inner workings of the control loops as much as possible with the knowledge acquired during the degree.

Introduction

Objectives

This project consists on a performance comparison of a series of grid synchronisation techniques under common network voltage faults. This subject has been previously studied in different ways by all sorts of research groups. However, the number of tests under which the control loops are to be studied provides a more detailed analysis of the dynamic performance of the designs under voltage faults.

The main objective of this project is to produce a performance report of the PLL designs under the faults and to determine which design is optimal under the different tested voltage faults. This analysis is to be used for future reference by the CITCEA researchers when simulating larger control loops of electric devices such as VSC transformers.

The following phases were followed in order to satisfy the afore mentioned objectives:

- The main types of voltage faults and the main mathematical concepts are introduced in Chapter 1
- The functioning principles of the various PLL designs are detailed in Chapter 2
- The voltage fault tests and other experimental procedures are explained in Chapter 3
- The results of the simulations are analysed in Chapter 4.

Scope of the Project

The scope of this project is to provide an understanding as to how well the studied PLL designs perform under certain types of voltage faults ubiquitous in distribution networks. The study of the optimal phase loop tunings has been excluded due to the variation of the parameters depending on the control loop the PLLs are contained in. Performance of the PLLs within larger systems has also been excluded due to the complexity that study would imply. Including control loops that make use of the PLL's outputs has also been considered out of the question, due to the specialised nature of this project.

1. Theory introduction

1.1 Basic Concepts

Before analysing and comparing the behaviour of the different PLL architectures, introducing a series of basic concepts is essential. In this section voltage wave behaviour and the applicable mathematical transforms used to define them will be detailed.

In order to proceed with the simulations, understanding a three-phase electrical network's proper behaviour and how this behaviour may deviate into alterations is very important. This chapter explains what to expect from an AC three-phase system in both balanced and unbalanced scenarios.

Ideally, an AC voltage wave input signal for an appliance should have constant amplitude, frequency and a perfect sinusoidal shape. However, this proves to be practically impossible in an actual practical situation.

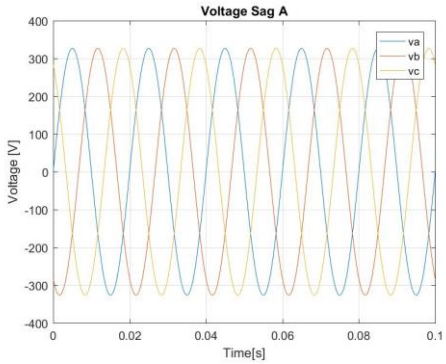


Figure 1.1 Balanced three-phase voltage signal

In the European continent, most distribution networks work at 50Hz and the highest fidelity signals can be found at the output of power generators. However, throughout the distribution network many different factors alter the AC voltage signal. Naturally, electrical demand is not constant throughout the day thus producing variations on the amount of power the generators must produce in order

to maintain the network's nominal values. It is important to note that demand includes all the customers connected to the network. For example, in mainland Spain and Balearic Islands this would involve all the users connected to the 50 Hz national network managed by "Red Eléctrica de España". From industrial customers such as SEAT or IVECO with enormous manufacturing plants to domestic users that power up appliances of all sorts. This is the reason for a non-linear demand curve that alters the wave characteristics of the voltage signal transported throughout the network.

Aside from the variations in demand, malfunctions in the distribution hardware can also produce disturbances. Transformers and livewires may go down for maintenance reasons and failures. These can break down producing short-circuits, increased resistance and even open the circuit preventing current from passing through them. This subject will be explained in more depth later in the project and is usually referred to as a voltage sag.

The afore mentioned cases tend to produce amplitude variations in the distribution. However, frequency variations of the voltage signal can also be produced by changes in demand. Should the supply capacity and the demand change abruptly, it could result in a frequency imbalance. This risk is minimised by interconnecting networks. The bigger the network the harder it is to find significant changes in frequency values. For example, the expected frequency variations in a domestic micro-grid are a hundredfold those found in a national distribution network.

The importance of control systems in the generation and distribution networks becomes blatant in order to maintain voltage wave quality standards. As can be seen, transient states occur at random intervals depending on the supply-demand factors and other imbalance causes inherent to the structure of the network. Efficient management of said control systems has a major impact on both the environmental and the economic aspects of the industry.

The following sections provide specific descriptions of the wide array of alterations the voltage signal undergo through.

1.2. Amplitude Considerations

The amplitude of the voltage wave has direct influence on the amount of power that load circuit consumes. Therefore, it is a variable that must remain within a certain tolerance limit in order to maintain or even enable performance of certain applications.

The manner in which voltage amplitude variations occur is very diverse, and this section details the main causes and behaviours of said variations.

In compliance with the current Spanish legislation [1] for electrical verifications and energy supply consistency, the tolerance limit for amplitude variations establishes that the variations should never exceed a +/- 7% of its reference value.

Causes of variations in voltage amplitude

The main cause for voltage amplitude variations resides in the variable nature of the equivalent impedance of the loads connected to the network. The variations in impedance are owed to the type of loads and their demand throughout the day.

For instance, a leisure centre will have a very high energy demand during the day where cinemas, bars, shops, etc. will be fully operational. Whereas at night, when the centre is closed, the same area will drop its demand to practically no power consumption whatsoever.

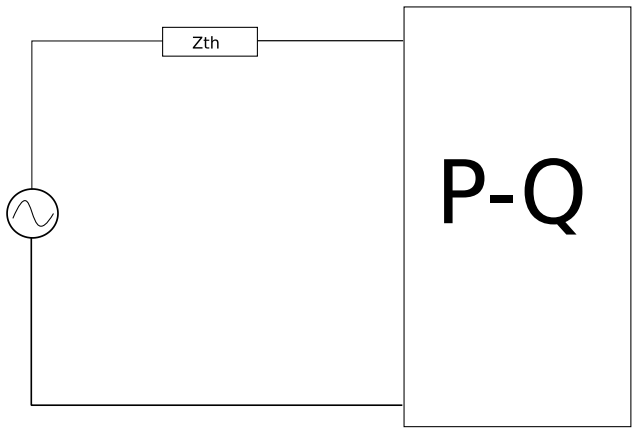


Figure 1.2 Thevenin Equivalent example representing Generation and Load of a network

The Thevenin equivalent circuit consists of two main parts. On the left hand side the generator represents the sum of all the systems that input power into the circuit and the impedance of all those systems. On the right hand side lies the impedance of the sum of loads that demand energy from the generation system. Taking into account that the load impedance varies greatly in a non-linear way, the generation system must be able to keep up with the fluctuations. This is also a solid demonstration for the need of efficient and fast control systems in a network.

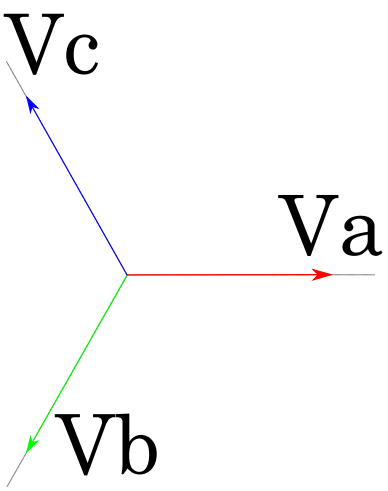
Aside from the causes associated to consumer-related impedance fluctuations, faults in hardware may also disrupt the amplitude and balance of three-phase networks. These faults are a consequence of an abrupt change in the impedance of the electrical transmission lines. Essentially due to a transmission fault and its propagation through a transformer.

1.3. Voltage Sags

The previously mentioned phenomena are known as voltage sags. They are classified according to the nature of the fault and the position where the voltage is measured relative to the transformers. Within this classification two main sets of voltage sags can be differentiated. Types A, B, C and E are all the main kinds of voltage sag that can be found by themselves whereas types D, F and G are the propagation of the first types through transformers [2].

Figures 1.3-1.6 and 1.8-1.10 illustrate the phasor sets for the different kinds of voltage sags. Equations 1.3.1-1.3.14 mathematically define the voltage sag. The odd equations show the phasors in Cartesian coordinates and the even equations show the voltage sags decomposed into positive, negative and zero sequence (the concept behind this decomposition is explained later in the chapter). The $D\overrightarrow{Vsa}^{+}$ is known as the "characteristic voltage" of a voltage sag. D is a scalar that corresponds to the depth of the voltage dip and $\overrightarrow{Vsa}^{+}$ is the amplitude of the voltage signal before the sag.

Voltage Sag **A**. Three-phase fault and three-phase-to-ground fault



$$\begin{bmatrix}\overrightarrow{Va}\\ \overrightarrow{Vb}\\ \overrightarrow{Vc}\end{bmatrix} = \begin{bmatrix}1\\ -\frac{1}{2}-j\frac{\sqrt{3}}{2}\\ -\frac{1}{2}+j\frac{\sqrt{3}}{2}\end{bmatrix} D\overrightarrow{Vsa}^{+} \quad (1.3.1)$$

$$\begin{bmatrix}\overrightarrow{Va}^{+}\\ \overrightarrow{Va}^{-}\\ \overrightarrow{Va}^{0}\end{bmatrix} = \begin{bmatrix}1\\ 0\\ 0\end{bmatrix} D\overrightarrow{Vsa}^{+} \quad (1.3.2)$$

Figure 1.3 Sag type A

Voltage Sag **B**. Single-phase-to-ground fault

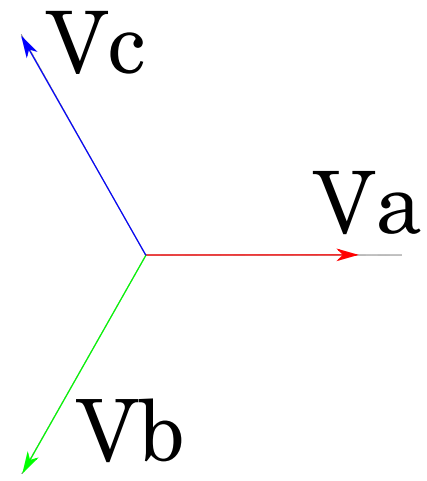
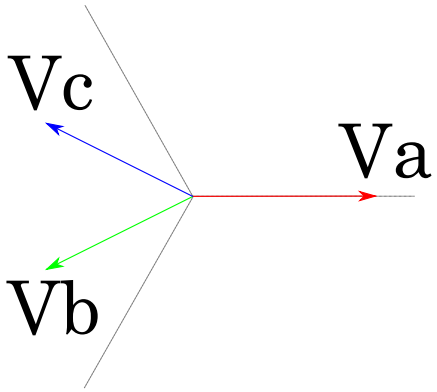


Figure 1.4 Sag type B

$$\begin{bmatrix}\overrightarrow{Va}\\ \overrightarrow{Vb}\\ \overrightarrow{Vc}\end{bmatrix} = \begin{bmatrix}D\\ -\frac{1}{2}-j\frac{\sqrt{3}}{2}\\ -\frac{1}{2}+j\frac{\sqrt{3}}{2}\end{bmatrix} \overrightarrow{Vsa}^{+} \quad (1.3.3)$$

$$\begin{bmatrix}\overrightarrow{Va}^{+}\\ \overrightarrow{Va}^{-}\\ \overrightarrow{Va}^{0}\end{bmatrix} = \begin{bmatrix}\frac{1}{3}(2+D)\\ -\frac{1}{3}(1-D)\\ -\frac{1}{3}(1-D)\end{bmatrix} \overrightarrow{Vsa}^{+} \quad (1.3.4)$$

Voltage Sag **C**. Phase-to-phase fault

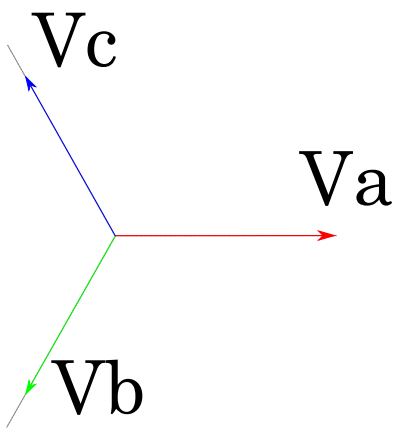


$$\begin{bmatrix}\overrightarrow{Va}\\ \overrightarrow{Vb}\\ \overrightarrow{Vc}\end{bmatrix} = \begin{bmatrix}1\\ -\frac{1}{2} - j\frac{\sqrt{3}}{2}D\\ -\frac{1}{2} + j\frac{\sqrt{3}}{2}D\end{bmatrix}\overrightarrow{Vsa}^{+} \quad (1.3.5)$$

$$\begin{bmatrix}\overrightarrow{Va}^{+}\\ \overrightarrow{Va}^{-}\\ \overrightarrow{Va}^{0}\end{bmatrix} = \begin{bmatrix}\frac{1}{2}(1+D)\\ \frac{1}{2}(1-D)\\ 0\end{bmatrix}\overrightarrow{Vsa}^{+} \quad (1.3.6)$$

Figure 1.5 Sag type C

Voltage Sag **E**. Two-phase to ground fault



$$\begin{bmatrix}\overrightarrow{Va}\\ \overrightarrow{Vb}\\ \overrightarrow{Vc}\end{bmatrix} = \begin{bmatrix}1\\ -\frac{1}{2}D - j\frac{\sqrt{3}}{2}D\\ -\frac{1}{2}D + j\frac{\sqrt{3}}{2}D\end{bmatrix}\overrightarrow{Vsa}^{+} \quad (1.3.7)$$

$$\begin{bmatrix}\overrightarrow{Va}^{+}\\ \overrightarrow{Va}^{-}\\ \overrightarrow{Va}^{0}\end{bmatrix} = \begin{bmatrix}\frac{1}{3}(1+2D)\\ \frac{1}{3}(1-D)\\ \frac{1}{3}(1-D)\end{bmatrix}\overrightarrow{Vsa}^{+} \quad (1.3.8)$$

Figure 1.6 Sag type E

As previously mentioned, there are three more kinds of voltage sags that are a consequence of the propagation through a transformer of the 4 primary sags. These voltage sags occur in specific points of the circuit depending on their relative position to the transformers. The following two cascade-connected Dy transformers power line diagram will be used to exemplify this occurrence.

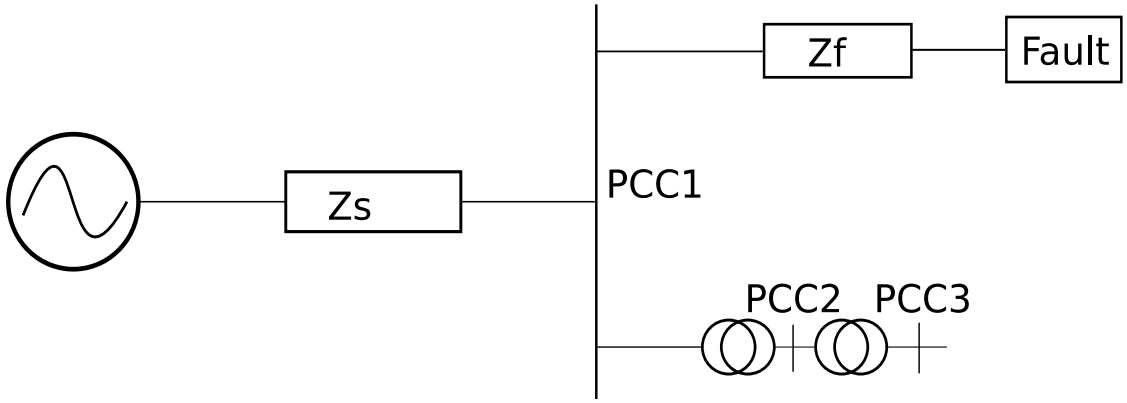


Figure 1.7 Voltage sag propagation along PCC1, PCC2 and PCC3 in a power line with two cascade-connected Dy transformers

Table 1.1 defines what sort of voltage sag occurs according to the point of common coupling in which the voltage is measured:

Fault type	PCC1	PCC2	PCC3
Three-phase/three-phase to ground	A	A	A
Single-phase to ground	B	C	D
Two-phase	C	D	C
Two-phase to ground	E	F	G

Table 1.1 Propagation of voltage sags through Dy transformers

Sag type **D**. Propagation of a sag type **C**

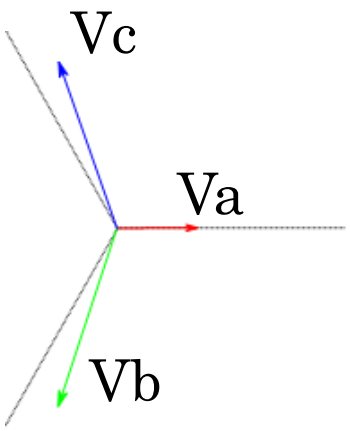


Figure 1.8 Voltage Sag D

$$\begin{bmatrix}\overrightarrow{Va}\\ \overrightarrow{Vb}\\ \overrightarrow{Vc}\end{bmatrix} = \begin{bmatrix} D \\ -\frac{1}{2}D - j\frac{\sqrt{3}}{2} \\ -\frac{1}{2}D + j\frac{\sqrt{3}}{2}\end{bmatrix}\overrightarrow{Vsa}^{+} \quad (1.3.9)$$

$$\begin{bmatrix}\overrightarrow{Va}^{+}\\ \overrightarrow{Va}^{-}\\ \overrightarrow{Va}^{0}\end{bmatrix} = \begin{bmatrix}\frac{1}{2}(1+D)\\ -\frac{1}{2}(1-D)\\ 0\end{bmatrix}\overrightarrow{Vsa}^{+} \quad (1.3.10)$$

Sag type **F**. Propagation of a sag type **E**

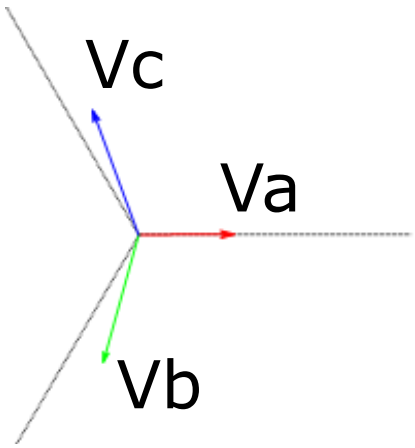
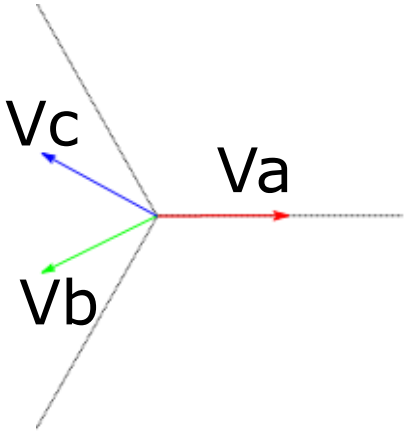


Figure 1.9 Voltage sag F

$$\begin{bmatrix}\overrightarrow{Va}\\ \overrightarrow{Vb}\\ \overrightarrow{Vc}\end{bmatrix} = \begin{bmatrix} D \\ -\frac{1}{2}D - j\frac{2+D}{\sqrt{12}} \\ -\frac{1}{2}D + j\frac{2+D}{\sqrt{12}}\end{bmatrix}\overrightarrow{Vsa}^{+} \quad (1.3.11)$$

$$\begin{bmatrix}\overrightarrow{Va}^{+}\\ \overrightarrow{Va}^{-}\\ \overrightarrow{Va}^{0}\end{bmatrix} = \begin{bmatrix}\frac{1}{3}(1+2D)\\ -\frac{1}{3}(1-D)\\ 0\end{bmatrix}\overrightarrow{Vsa}^{+} \quad (1.3.12)$$

Sag type **G**. Propagation of a sag type **F**



$$\begin{bmatrix}\overrightarrow{Va}\\ \overrightarrow{Vb}\\ \overrightarrow{Vc}\end{bmatrix} = \begin{bmatrix}\frac{1}{3}(2+D)\\ -\frac{2+D}{6} - j\frac{\sqrt{3}}{2}\\ -\frac{2+D}{6}D + j\frac{\sqrt{3}}{2}\end{bmatrix}\overrightarrow{Vsa} \quad (1.3.13)$$

$$\begin{bmatrix}\overrightarrow{Va}^{+}\\ \overrightarrow{Va}^{-}\\ \overrightarrow{Va}^{0}\end{bmatrix} = \begin{bmatrix}\frac{1}{3}(1+2D)\\ \frac{1}{3}(1-D)\\ 0\end{bmatrix}\overrightarrow{Vsa}^{+} \quad (1.3.14)$$

Figure 1.10 Voltage sag G

The D variable is considered a constant in this project. In some other cases, the D variable can be defined as a phasor thus producing much more complex voltage sag effects by modifying the phase of all the resulting signals. Implementation of the D variable as a vector enables the definition of much more complex voltage disruptions. However, analysis of PLL behaviour in such complex scenarios becomes irrelevant in this project.

1.4. Frequency Considerations

The frequency of an electrical AC system is directly related to the rotation speed of the alternators that generate it. This rotation speed must be the same for all generators within the same network for its adequate performance and synchrony.

This frequency value fluctuates with the ratio between supply and demand. Generators work at a higher capacity than the average demand, saving the surplus energy in form of mechanical rotation. This surplus energy is stored in order to absorb peaks in electrical demand. However, at certain times this system is unable to compensate the imbalance between supply and demand thus making the generators vary their rotation speed. This results in a frequency variation that can be perceived throughout the whole network.

Should the system load be lower than the energy generation rate, the generators tend to slow down lowering the network's frequency. This issue is addressed by means of a breaking system that absorbs the excess energy and forces the generators to rotate at the adequate speed.

On an opposite scenario, should there be a peak in demand, the generation system tries to compensate the difference with the surplus energy that is stored in mechanical form. If the surplus energy is not enough for the generators to compensate the demand peak, then their rotation speed increases.

Taking into account both scenarios, a higher number of generators implies that compensation of significant electrical demand changes lessens the impact on the frequency values of the network.

A certain degree of frequency variation is considered both acceptable and inevitable due to the fluctuating nature of the demand curve. The following values provide an insight as to how much frequency can in a synchronous vary throughout the time domain:

- 50 Hz ± 1 % (49.5...50,5 Hz)On average 99,5 % yearly.
- 50 Hz -6%, +4% (47...52 Hz) On average 100 % of the time.

1.5. Harmonics

Harmonic distortion is a phenomenon that alters the shape of a purely sinusoidal signal. Distorted signals can have severely deformed shapes in comparison with the original signal. These distortions consist on the superposition of sinusoidal signals of frequencies several times that of the original signal. The only efficient way of studying this kind of wave-form alteration is by means of a frequency analysis [3]. The Fourier transform enables the mathematical definition of a non-sinusoidal signal by decomposing it into a sum of perfect sine waves with different frequencies and amplitudes. The following example illustrates the way in which this mathematical tool works:

Equation 1.5.1 shows the generic expression of an oscillating signal decomposed into sinusoidal waves of different frequencies and amplitudes:

$$Q(t) = A_1\sin(t \cdot \omega_1) + A_2\sin(t \cdot \omega_2) + A_3\sin(t \cdot \omega_3) + A_4\sin(t \cdot \omega_4) \quad (1.5.1)$$

Equation 1.5.2 shows the expression for a voltage wave with 3rd 5th and 7th harmonics

$$Q(t) = V_1\sin(\omega t) + V_3\sin(3\omega t) + V_5\sin(5\omega t) + V_7\sin(7\omega t) \quad (1.5.2)$$

Usually, the amplitudes for the different harmonics derived from the fundamental frequency signal are expressed in a percentage:

$$V_n(\%) = \frac{V_{nth\ harmonic}}{V_{fundamental}} \cdot 100 \quad (1.5.3)$$

According to UNE-EN 50160 [1], 95% of the mean values for the amplitude of the different harmonics measured in 10 min periods may not surpass those of the following table.

Even Order		Odd Order			
		Not multiples of 3		Multiples of 3	
Order	Amplitude limit(%	Order	Amplitude limit(%)	Order	Amplitude limit(%)
2	2%	5	6%	3	5%
4	1.00%	7	5%	9	1.50%
6	0.50%	11	3.50%	15	0.50%
8	0.50%	13	3%	21	0.50%
10	0.50%	17	2%		
12	0.50%	19	1.50%		
14	0.50%	23	1.50%		
16	0.50%	25	1.50%		

Table 1.2 Permitted relative Harmonic amplitude values for Voltage signal according to UN50160-EN

The total harmonic distortion parameter or THD is an indicator as to how much harmonics have modified a signal. It can be calculated as:

$$THD(\%) = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + \cdots}}{V_1} \quad (1.5.4)$$

The UNE-EN 50160 also establishes that the Total Harmonic Distortion (THD) for the signal may never surpass the 8% value.

Usually, the elements that connect to the grid demand a linear amount of energy. However, certain appliance demand non-sinusoidal inputs thus generating current and voltage harmonics that flow throughout the network. These non-linear demands can come from TV sets, Personal Computers, Arc furnaces, electronic control units, etc.

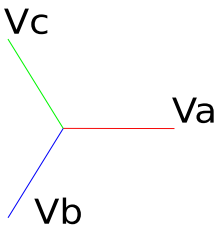
The effects harmonics produce on a signal are very different depending on the order of the frequency:

- When the order of the harmonic is even, the harmonic distortion does not produce imbalances in the phasor set. Therefore, this kind of harmonic distortion only introduces positive sequence into the system.
- When the order of the harmonic is odd but not multiple of 3, the harmonic distortion produces imbalance in the phasor set. Therefore, this kind of harmonic distortion introduces negative sequence into the system.
- When the order of the harmonic is odd and multiple of 3, the harmonic distortion introduces homopolar component into the system. This implies that the sum of the 3 phases no longer will be 0. Controlling this issue is really complicated for PLLs.

1.6. Mathematical Transforms

In order to comprehend the complete functionality of a PLL architecture, certain mathematical concepts must be introduced. These tools simplify greatly operation with three phase sinusoidal voltage signals both in balanced and in unbalanced scenarios.

The following figures illustrate the definition of a balanced three-phase voltage signal



$$\begin{bmatrix} Va \\ Vb \\ Vc \end{bmatrix} = V_{ABC} = \begin{bmatrix} 230\angle 0º \\ 230\angle -120º \\ 230\angle 120º \end{bmatrix} \qquad (1.6.1)$$

Figure 1.11 Balanced Voltage phasor set

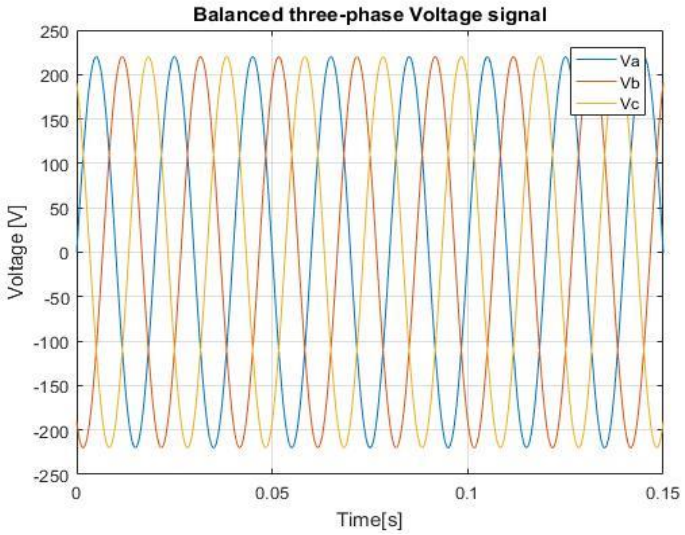


Figure 1.12 Balanced three-phase voltage signal amplitude [V], time[s] graph

As can be seen, the figure1.11 shows 3 vectors that are equal in modulus and are 120 degrees apart between them. Upon analysis of the time amplitude graph, three sinusoidal waves can be found oscillating with a 120-degree phase difference between them.

The phasors represent the voltage vector modulus and the initial phase. The angular position (phase) of the resulting vector increases with time in relation to its frequency. Therefore, the phasor diagram can in fact be understood as an isometric projection of the initial voltage vectors.as a function of time. Hence, the frequency can be seen as the rotation on the isometric plain of the vector composed by (Va, Vb, Vc). Figure 1.13 illustrates this:

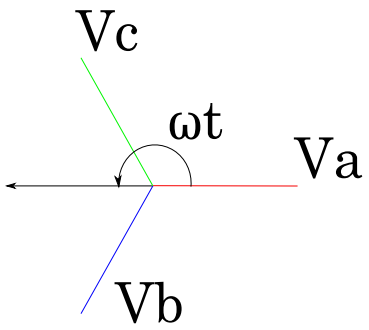


Figure 1.13 Complex voltage vector rotation

Clarke Transform

Since mathematical operations with three out of phase sine waves are not trivial and the afore mentioned sine waves can be plotted in a phasor diagram, the Clarke transform proposes the use of a geometrical solution to simplify the signal analysis.

Upon inspection of the previously included balanced three phase diagram, three phasors with a 120-degree angle between them can be seen. Such phasor diagram represents the three AC voltage oscillations in canonical form.

The Clarke transform proposes a basis change in which the phasors no longer form 120-degree angles between them. Instead, two phasors form a 90-degree angle between them and the third is perpendicular to the x-y axes like so:

$$\begin{bmatrix} V\alpha \\ V\beta \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \frac{2}{3} \begin{bmatrix} Va \\ Vb \\ Vc \end{bmatrix} \quad (1.6.2)$$

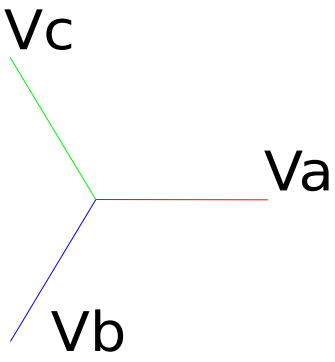


Figure 1.14 Phasor set before the Clarke Transform

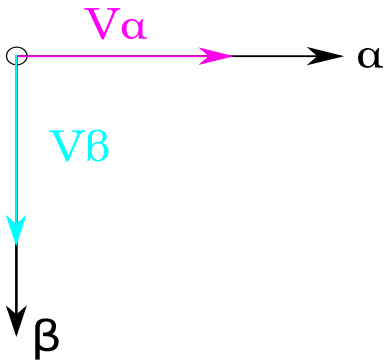


Figure 1.15 αβ Frame after Clarke Transform

Upon application of the transform, the output shows two identical sine waves with a 90º phase shift between them and a 0 constant corresponding to the perpendicular.

The Park Rotation

The Clarke transform greatly simplifies operations on the voltage signals. However, it is with the Park rotation that simplification is hugely increased. The rotation essentially consists on rotating the basis of the phasor diagram in sync with the pulsing frequency of the voltage phasors. By doing so, instead of working with sine waves the voltage signals are linearized thus enabling easier analysis.

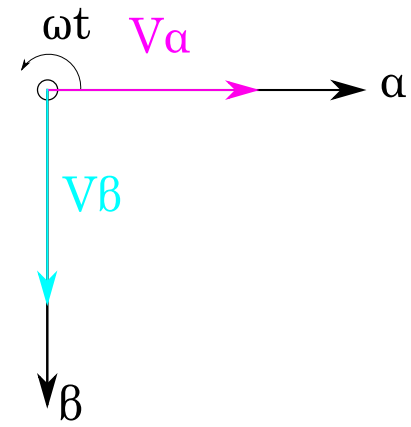


Figure 1.16 αβ Frame with the rotation

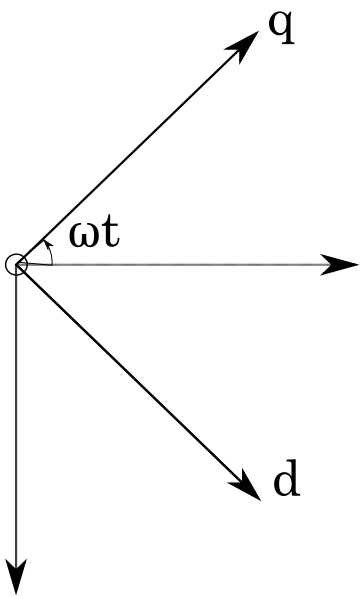


Figure 1.17 dq Frame after Park rotation

As can be seen, the in fig 1.16, the dq frame rotates in synchrony with the voltage vectors outputting constant values in the steady state. Working with constant values is ideal in order to ease control of any given system. The Park rotation is a central part in most phase locked loop architectures due to its advantages.

In order to apply the rotation, the output vector from the Clarke transform is multiplied by a simple rotation matrix. Naturally, the angle of the voltage signal must correspond to the angle within the matrix.

$$\begin{bmatrix} Vq \\ Vd \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V\alpha \\ V\beta \end{bmatrix} \quad (1.6.4)$$

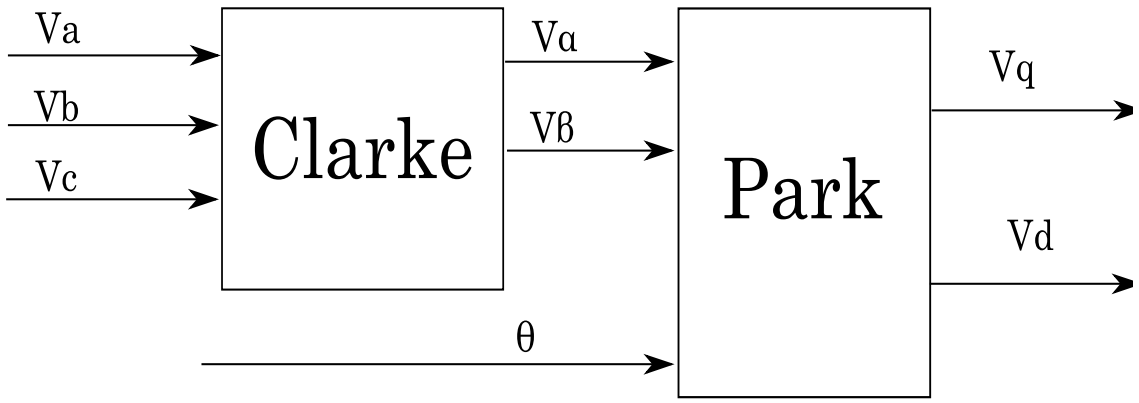


Figure 1.18 Overview of the Clarke and Park Transformation and the input and output signals

The different variables and the transformation that produces them can be seen in fig 1.18.

This is a fairly easy task in balanced systems. However, in unbalanced systems certain issues arise. Before understanding the problems associated to the application of the park rotation to imbalanced voltages, the Fortesque transform must be introduced.

Fortescue Theorem

The Fortescue transform is a decomposition of a set of N unbalanced phasors into a sum of N sets of balanced phasors. Applied to electrical engineering, this means that any unbalanced three-phase system can be expressed as the sum of three balanced three-phase systems.

The three balanced sets that will serve as a basis to compose any given three-phase system is formed by the positive sequence set, the negative sequence set and the zero sequence. Fig 1.19 shows the

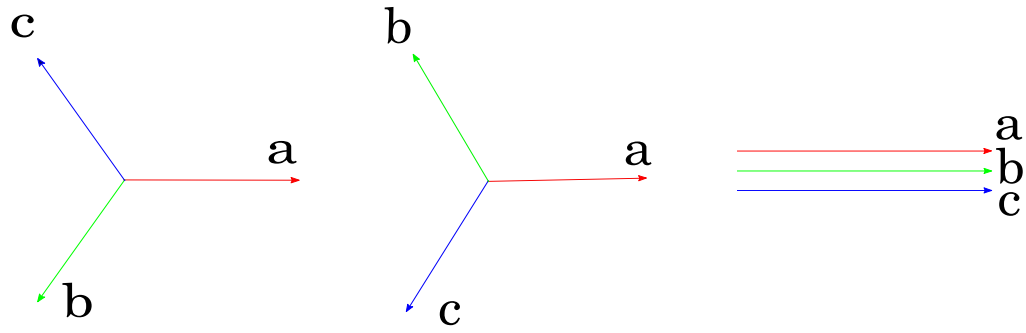


Figure 1.19 Components into which the Fortescue transform decomposes the three-phase vector: Positive sequence, Negative sequence and homopolar.

The positive and negative sequence phasor sets rotate in opposite directions at the same frequency. This implies that an unbalanced three phase system does not have a unique angular rotation and therefore applying a Park rotation to the unbalanced system will not result in a constant value.

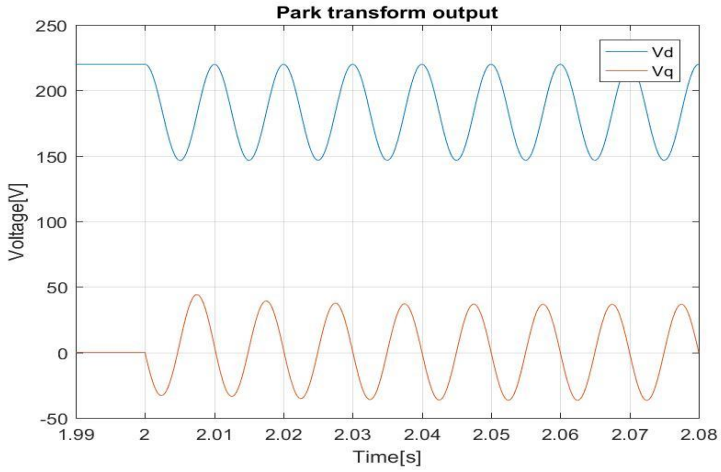


Figure 1.20 100 Hz ripple found in a dq voltage frame under unbalanced voltage input signal

As can be seen in Fig 1.20, after applying the park rotation to the unbalanced three phase voltage input the Vq and Vd voltages have a 100Hz oscillating component.

This is due to the fact that the park rotation has been applied with a 50 Hz frequency and the negative sequence component of the unbalanced entry voltage rotates at the same frequency in the opposite direction.

The actual mathematical transformation that decomposes the unbalanced system into three balanced sets of phasors is not actually relevant to this project since the studied PLL architectures do not actually use the transform. However, the implications of the existence of positive and negative sequences is pivotal on a qualitative level.

2. The Phase locked Loop

The Phase Locked Loop or PLL is a control system that tracks and outputs the phase of a given input signal. It's application in electrical engineering is essential due to the fact that in most cases the phase is used in mathematical transforms to make voltage signal analysis more tractable.

There are various types of designs and architectures for a very wide range of applications. Since trying to cover the whole spectrum of PLL designs for electrical signal phase tracking is not feasible, a small selection of them will be introduced later on.

In any case, certain design aspects are common amongst the majority of the PLL catalogue. In electrical engineering, most if not all the PLL designs imply a negative feedback control system formed by 3 components; a Phase Detector (PD), a Filter and a Voltage controlled Oscillator (VCO).

-Phase Detector (PD): The PD converts the angle difference between the reference angle and the output from the VCO into a voltage. This voltage is used to control the VCO's output.

-Filter: The filter has two main functions.

Firstly, it has a huge impact in the dynamic response of the loop. The speed at which steady state behavior is achieved is determined by the nature of the loop, which also has direct implications in the stability of the PLL.

Secondly, the filter is responsible for setting a limit to the oscillations in the voltage associated to the PD. In high voltage electrical applications, filters are usually low pass. They enable the attenuation of voltage harmonics and other frequency disruptions.

-Voltage Controlled Oscillator:

The VCO is a device that produces a wave signal frequency of which is related to a voltage input.

Nevertheless, in this project the physical representation and implementation of these components is not taken into consideration. The scope of this project reduces these designs to their transfer functions.

2.1 Studied PLL designs

Out of the wide selection of available PLL designs only 6 were compared in this project for a series of reasons.

Firstly, tracking the phase of a signal is necessity in many applications, most of which are completely unrelated to the main objective of this project. Therefore, the studied PLL designs are mainly used to track the phase of three-phase voltage signals found in distribution networks.

Secondly, the main idea is to simulate their performance in continuous Laplace space and therefore those designs which rely on discrete control and are used in DSP (Digital Signal Processor) implementation are excluded.

Finally, some other designs were excluded due to the difficulties encountered in the numerical simulation. The information used in order to produce the Simulink models comes from diverse publications in the IEEEXPLORE library and the results obtained from simulating some designs was clearly inaccurate and unsatisfactory. Studying how well the PLL designs perform under faults is the main focus of this project. However, no matter how small the error can be during the fault, if the PLL is not capable of regaining normal operation then it was deemed irrelevant for the study.

2.1.1. Synchronous Reference Frame

The SRF-PLL (Synchronous Reference Frame PLL) is the simplest design to be studied in this project. The three-phase voltage signal is transformed from abc to dq reference by means of the Clarke and Park matrices. The angular position of the reference frame is controlled by a feedback loop that fixes the value of Vq at 0. The difference between Vq and 0 is filtered by a PI controller. Integration of the output of the filter produces the voltage wave's phase. [4]

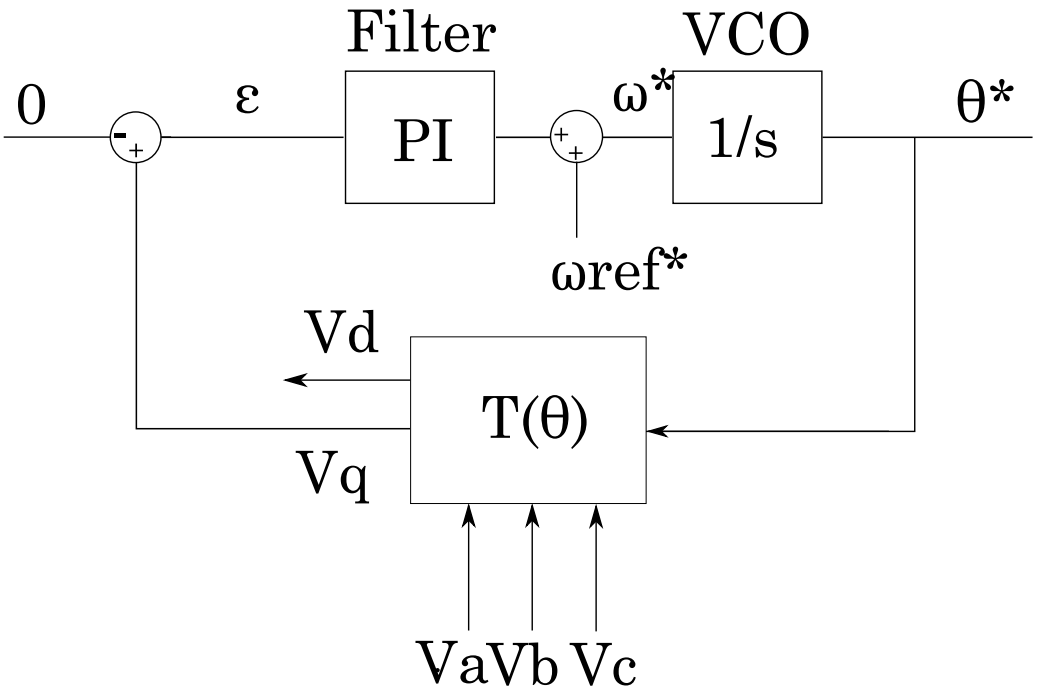


Figure 2.1 SRF-PLL Structure Block Diagram

The Vd and Vq frame is obtained from:

$$\begin{bmatrix} Vd \\ Vq \end{bmatrix} = \begin{bmatrix} \cos(\theta^*) & -\sin(\theta^*) \\ \sin(\theta^*) & \cos(\theta^*) \end{bmatrix} \cdot \frac{2}{3} \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \cdot Vm \cdot \begin{bmatrix} \cos(\omega t) \\ \cos(\omega t - \frac{2\pi}{3}) \\ \cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} \quad (2.1.1)$$

The voltage of interest is Vd which can be expressed as:

$$Vd = -Vm \cdot \sin(\theta - \theta^*) = e \quad (2.1.2)$$

The angular frequency can be defined as:

$$\omega^* = \frac{d\theta^*}{dt} = K_{loop} \cdot e \quad (2.1.3)$$

The controller is in charge of adjusting ω^* to a value close enough to that of the frequency of the voltage input in order to minimise the difference between the real phase and the estimated phase. Upon reaching a small enough phase difference, Vq will be 0 and therefore the angular frequency will stabilise.

There are two slight variations within the SRF-PLL. As can be noticed in the diagram, a feedforward with a ωref* parameter is included. In some implementations this parameter is set to 0 and in others, if the Vabc frequency is known to be around a certain value, the parameter is used to initialise the PLL. The feedforward can, if used correctly, improve the PLL's transient behaviour. Both Variations will be studied in the posterior comparison.

As can be extracted from the diagram, the output of the PLL θ* is the estimation of the dq rotating frame's angular position. Under correct operation the difference between the estimation and the real angular position should be small enough to ensure negligible deviations of the Vq signal. As explained previously, when the Park transform rotates at a different rate from the 50Hz frequency of the network, oscillations in the Vq and Vd values can be observed. If the filter is capable of attenuating these oscillations the error in the PLL output is very small and thus the tuning of the bandwidth of the PI controller has a great impact on the performance of the SRF-PLL. The PI acts as a form of low-pass filter

Upon understanding the issue with the scenarios in which the Vq value differs from 0, the effect of voltage sags and other Vabc disruptions has on the phase estimation becomes blatant. This PLL excels in its design simplicity but it lacks the capacity to minimise the error when the voltage input signal is unbalanced.

2.1.2. Double Decoupling Synchronous Reference Frame

The DDSRF-PLL or decoupled double synchronous frame PLL is an evolution of the SRF-PLL. Essentially, instead of using a single park rotation with the positive sequence, what it does it that it used to dq frames rotating in opposite directions, taking into account the negative sequence of the voltage input. The dq+ and dq- voltages are decoupled and used to correct the 100Hz ripple product of unbalanced three-phase inputs. The decoupling system enables the PLL to stabilise under unbalanced conditions making it much more accurate during voltage sags. [5]

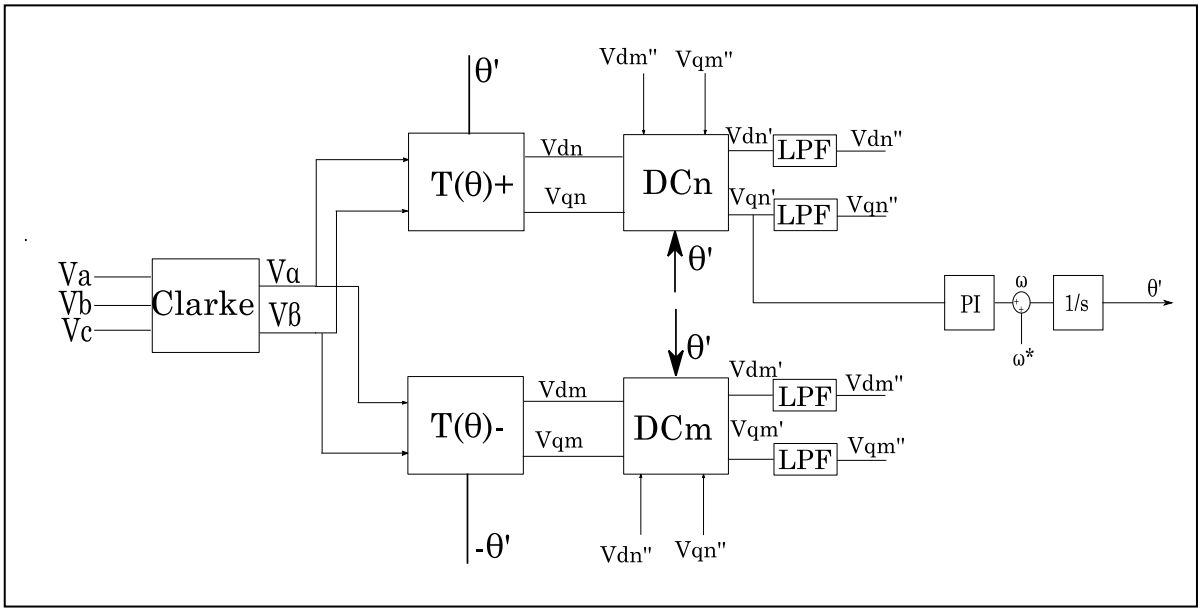


Figure 2.2 DDSRF-PLL Structure Block diagram

Figure 2.2 shows the block diagram for the DDSRF-PLL.

The DDSRF is a synchronous reference frame PLL that relies on a PI controller to maintain the Vqn' variable at 0 just like in the SRF design. In this case, the feedforward is essential in the initial transient state. Should the feedforward not be an accurate approximation of the grid frequency, the PLL would destabilise almost immediately.

The m and n parameters are set to -1 and 1 respectively. The n parameter is associated to the positive sequence and the m is associated to the negative sequence. The DC or decoupling block subtracts the interference of the negative sequence found in the positive dq frame and viceversa. The decoupling block is presented in the following diagram:

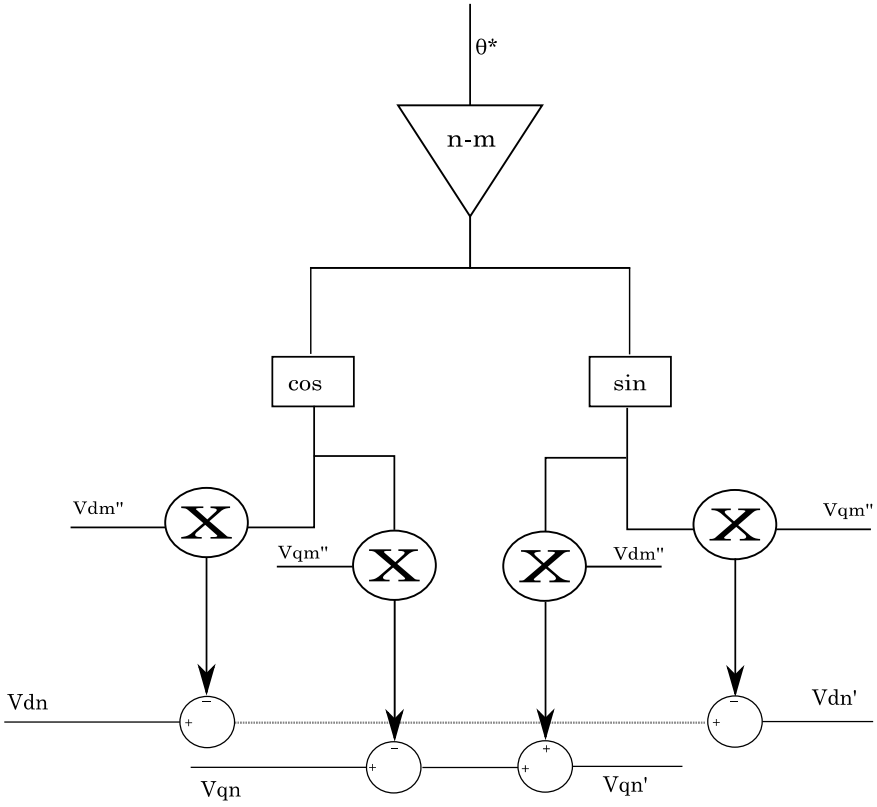


Figure 2.3 Positive sequence decoupling block

The equations of the positive and negative sequence dq frames are defined as:

$$Vdq^{+} = \begin{bmatrix} Vd^{+1} \\ Vq^{+1} \end{bmatrix} = V^{+} \begin{bmatrix} \cos(\emptyset^{+1}) \\ \sin(\emptyset^{+1}) \end{bmatrix} + V^{-1} \begin{bmatrix} \cos(2\omega t) & \sin(2\omega t) \\ -\sin(2\omega t) & \cos(2\omega t) \end{bmatrix} \begin{bmatrix} \cos(\emptyset^{-1}) \\ \sin(\emptyset^{-1}) \end{bmatrix} \quad (2.1.4)$$

$$Vdq^{-} = \begin{bmatrix} Vd^{-1} \\ Vq^{-1} \end{bmatrix} = V^{-} \begin{bmatrix} \cos(\emptyset^{-1}) \\ \sin(\emptyset^{-1}) \end{bmatrix} + V^{+1} \begin{bmatrix} \cos(2\omega t) & \sin(2\omega t) \\ -\sin(2\omega t) & \cos(2\omega t) \end{bmatrix} \begin{bmatrix} \cos(\emptyset^{+1}) \\ \sin(\emptyset^{+1}) \end{bmatrix} \quad (2.1.5)$$

The $\emptyset^{+1}$ and $\emptyset^{-1}$ variables represent the phase difference between the angle output of the PLL and the real angular position of both positive and negative sequence. Since the Fortescue theorem enables the definition of an unbalanced set of 3 phasors by combination

of 3 balanced sets of phasors, the positive and negative sequence phasor sets are defined so that their rotation occurs at the same rate with opposite directions.

Therefore $\theta^{+} = -\ \theta^{-}$.

The decoupling block includes a Parke rotation applied to the 100 Hz ripple caused by the positive sequence component on to the negative sequence dq frame. The different components outputted by this 2ω rotation are subtracted accordingly to the positive sequence dq transform. This is the key to the DDSRF's capability to correct the phase calculation under unbalanced situations.

The low pass filter is used to attenuate the interferences that the decoupling block is not capable of correcting. Adjustment of its parameters greatly affects the dynamic behaviour of the PLL. The low pass filter used in simulation is a first order filter with the following transfer function[4]:

$$LPF(s) = \frac{\omega_f}{s + \omega_f} = \frac{1}{Ts + 1} \quad (2.1.6)$$

According to reference Grid Converters for Photovoltaic and Wind Power Systems, a very reasonable trade-off between time response and oscillation damping can be achieved by setting to $\omega_f = {}^{\omega}/_{\sqrt{2}}$.

2.1.3. Alfa Beta

The AB-PLL a stationary reference frame architecture that does not make use of the Park rotation. This PLL relies on basic trigonometry and the Clarke transform. [6]

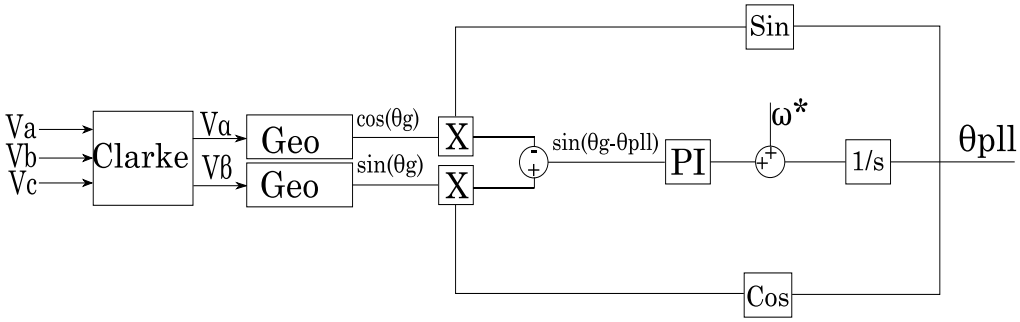


Figure 2.4 AB-PLL Block Diagram

This stationary reference frame PLL design makes use of trigonometric functions in order to determine the phase of the voltage input.

The following equations define its structure:

$$cos(\theta_g) = \frac{V\alpha}{\sqrt{V\alpha^2 + V\beta^2}} \quad (2.1.7)$$

$$sin(\theta_g) = \frac{V\beta}{\sqrt{V\alpha^2 + V\beta^2}} \quad (2.1.8)$$

Where θ_g is the real angular position of the voltage input. If $\emptyset = \theta_g - \theta_{PLL}$ is very small:

$$\emptyset = \theta_g - \theta_{PLL} \approx sin(\theta_g - \theta_{PLL}) \quad (2.1.9)$$

$$sin(\emptyset) = sin(\theta_g - \theta_{PLL}) = sin(\theta_g)cos(\theta_{PLL}) - cos(\theta_g)sin(\theta_{PLL}) \quad (2.1.10)$$

The closed loop control of the AB-PLL forces the ∅ value to 0 by means of a PI controller [5]. Under balanced conditions the performance of this PLL is expected to be comparable to that of the SRF-PLL. While the values of $V\alpha$ and $V\beta$ are the same, the value of $sin(\theta_g - \theta_{PLL})$ will be 0. However, should their be a voltage imbalance, the value of $sin(\theta_g - \theta_{PLL})$ *will oscillate* at 100 Hz. As with other PLL architectures, this design is incapable of dealing with the negative sequence oscillation component.

2.1.4. Dual Second Order Generalised Integrator

The DSOGI-PLL (Dual Second Order Generalised Integrator PLL) relies on adaptative filters based on the second order generalised integrator to apply an instantaneous symmetrical components method [7]. The SOGI structure acts as a phase detector and is applied to both Vα and Vß.

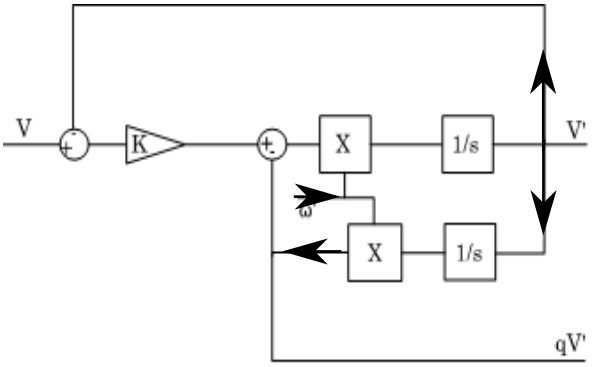


Figure 2.5 Second order generalised integrator block

The SOGI structure is an adaptive filtering architecture that outputs 2 signals with a 90-degree phase shift between them. The SOGI filter essentially acts as a band pass filter that greatly attenuates harmonic interference if tuned properly. If working under disturbances that affect the voltage frequency input, and should that frequency be out of the bandpass capability of this PLL, then the stability of the PLL would be completely compromised. Therefore, tuning of this architecture must allow some slack when operating under conditions of this kind. The k gain is responsible for the frequency adjustment of the filter. In theory, if set to the correct value, the DSOGI should behave similarly to the DDSRF design. In practice however, the dynamic response of the DSOGI is quite different.

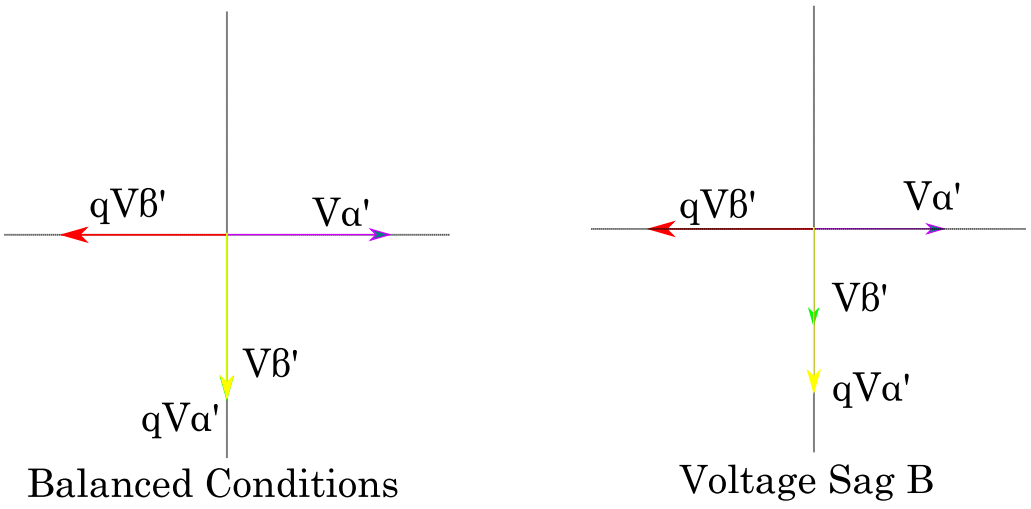


Figure 2.6 SOGI Filter outputs for balanced and Sag B scenarios

In figure 2., outputs of both SOGI filters can be seen under balanced voltage conditions and under a B type voltage sag (1 phase to ground fault).

The signals are then fed into the positive sequence converter block which creates a new Vα" and Vβ" which will have the same amplitude in steady state. This is what makes this PLL so precise under unbalanced conditions:

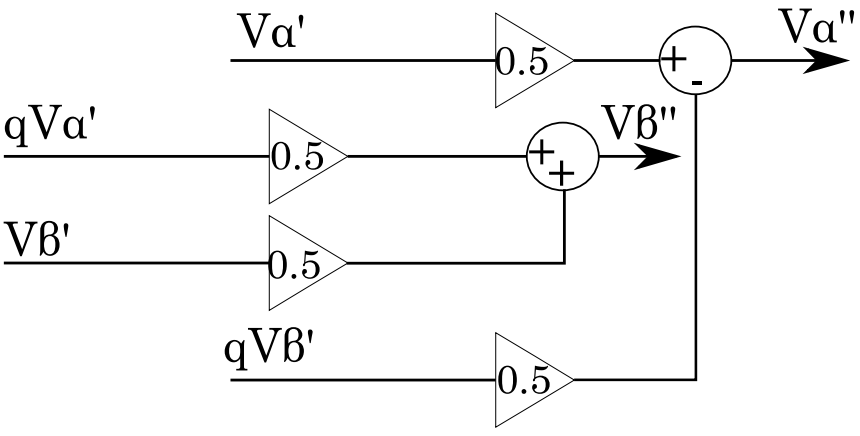


Figure 2.7 Positive sequence Converter block

The new Vα" and Vß" are fed into an SRF-PLL thus outputting the phase angle:

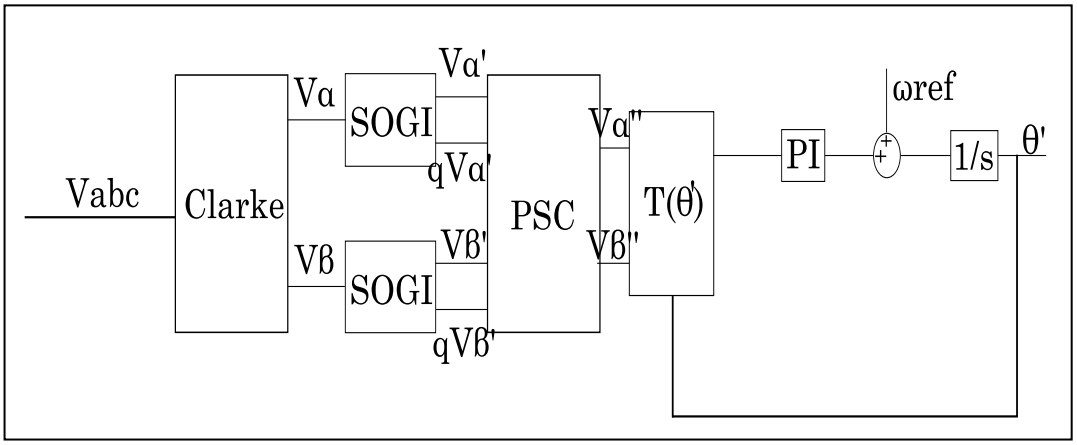


Figure 2.8 DSOGI-PLL block diagram

The following expressions are the transfer functions of the SOGI block:

$$D(s) = \frac{v'}{v}(s) = \frac{k\omega'}{s^2 + k\omega' s + \omega'^2} \quad (2.1.11)$$

$$Q(s) = \frac{qv'}{v}(s) = \frac{k\omega'^2}{s^2 + k\omega' s + \omega'^2} \quad (2.1.12)$$

Equations 2.1.11 and 2.1.12 define D(s) and Q(s) as the transfer functions of the SOGI quadrature signal generators. The k gain is a constant that will impact the dynamic response of the PLL. It is basically used to tune the damping of the transient state.

$$V''_{\alpha\beta} = [T^+_{dq}]V_{\alpha\beta} = \frac{1}{2}\begin{bmatrix} D(s) & -Q(s) \\ Q(s) & D(s) \end{bmatrix} V_{\alpha\beta} = \frac{1}{2}\frac{k\omega'}{s^2 + k\omega' + \omega'^2}\begin{bmatrix} s & -\omega' \\ \omega' & s \end{bmatrix} V_{\alpha\beta} \quad (2.1.13)$$

The new $V''_{\alpha\beta}$ values are used as an input for an SRF-PLL which will be much more stable under voltage disturbances with negative sequence component.

2.1.5. Double Alfa Beta

The DAB-PLL or Hybrid DDSRF-PLL is a combination of two of the previously introduced designs. Initially, the signal is fed into the same decoupling system as the DDSRF design. Once the interferences produced by the negative sequence has been filtered out from the positive sequence, the signal is fed into an inverse park transform. The output of the inverse park transform is an alfa beta signal that is used as an input for a regular AB-PLL design.[8]

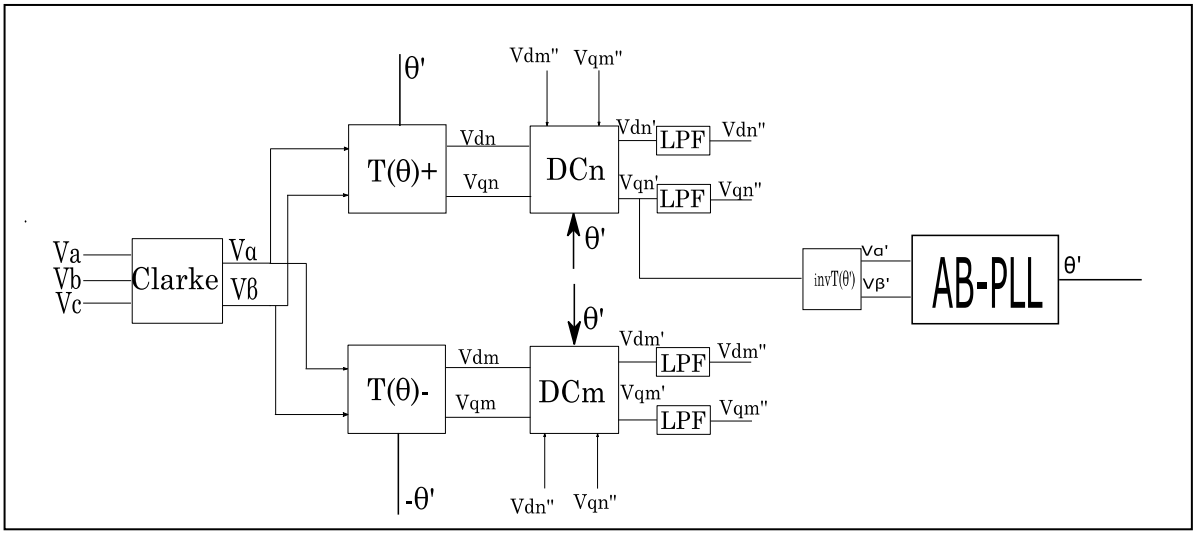


Figure 2.9 DAB-PLL Block diagram

Therefore, this system is essentially a pre-filtered AB-PLL that is capable of withstanding unbalanced voltage inputs. This design is a serious improvement over both the DDSRF and the AB PPLs, lowering the overshoot and oscillation of the response [8] throughout the tests that will be presented in the following chapters.

This PLL combines the strengths of the AB and DDSRF architectures. The main drawback the DDSRF has is its high frequency overshoot due to its synchronous reference frame design. This issue is bypassed by using synchronous techniques to filter the signal and stationary reference techniques to estimate the phase of the voltage input. Using stationary reference phase estimation greatly reduces the frequency overshoot mainly due to the fact that the frame has no frequency and therefore the error does not stack.

2.1.6. Discarded PLL designs

Initially, the idea was to include many more PLL architectures into this project but as previously explained, many were discarded. In this section some of those designs are briefly explained for future reference should this study be retaken.

- dq-CDSC PLL (dq-Frame Cascaded Delayed Signal Cancelation PLL); it makes use of cascaded notch filtering techniques before feeding the filtered signal into an SRF-PLL [9] .

- MAF-PLL or Moving Average Filter; This design makes use of the moving average filter alongside with the usual loop filter of an SRF-PLL. If certain conditions hold, the MAF is expected to perform as a perfect low-pass filter thus severely attenuating harmonics in the input [10].

- FFT-PLL (Fast Fourier Transform PLL); This design uses the fast Fourier transform to determine the frequency of the voltage input which is then integrated to produce the phase output. The signals are compared with reference sine and cosine waves and uses a ring buffer to filter out harmonics [11].

- LPN-PLL (Low Pass Notch Filter); This design, based on the FFT, uses a Notch filter centered at 100 Hz in substitution of the ring buffer [12].

- EPLL (Enhanced PLL); this design uses a non-linear synchronization technique where the sine of the phase output is fed back into the phase detector providing a more accurate definition of the error [6].

- QPLL(Quadrature PLL): The quadrature PLL is based on estimating in-phase and quadrature-phase amplitudes of the fundamental component of the input signal [6].

As mentioned previously, due to difficulties in tuning the architectures and finding up to par performance, or the discrete nature of some of these designs, they were excluded.

3. Experimental procedure

In order to compare the behaviour of the various PLL architectures presented in the previous chapter, a series of tests were designed. The benchmark process consists of Thirteen different three-phase voltage signals which will be used as an input to the different PLLs. These tests will enable the study of the dynamic behaviour of the PLLs in the transient state.

The main idea is to succeed in providing an insight as to how each control loop reacts and adapts to the most widespread voltage faults introduced in previous chapters. The tests will include the main types of voltage sags, a $\frac{\pi}{2}$ phase jump, a positive and negative frequency variation and distorted input signals (harmonics).

In every test, the input will begin as a perfectly balanced 230 volt three-phase system. At the 2 second mark the variation will be introduced up until the 4 second mark where the input signal will return to its original balanced status. Studying both transitions is important because some PLLs will be able to balance the error under the fault and others will not be able to cope with it. The PLLs incapable of reducing the error during the fault will be able to return to correct functionality after the 4 second mark as will be seen in the results section.

From t=0 to t=2s and from t=4s onwards, the input signal is the same in all tests:

$$V_{ABC} = \begin{bmatrix} 230\angle 0º \\ 230\angle -120º \\ 230\angle 120º \end{bmatrix}$$

All of the voltage sag tests have been conducted with the D parameter set at 0.5 and $\overrightarrow{Vsa}^{+} = \frac{400}{\sqrt{3}} \cdot \sqrt{2}$ [V].

According to [13] voltage sags cannot last for longer than 250ms. However, for our analysis, using a 2s voltage sag does not alter the results of the testing and is a much more comfortable value.

3.1. Voltage sag test A

$$V_{ABC} = \begin{bmatrix} 115\angle 0º \\ 115\angle -120º \\ 115\angle 120º \end{bmatrix}$$

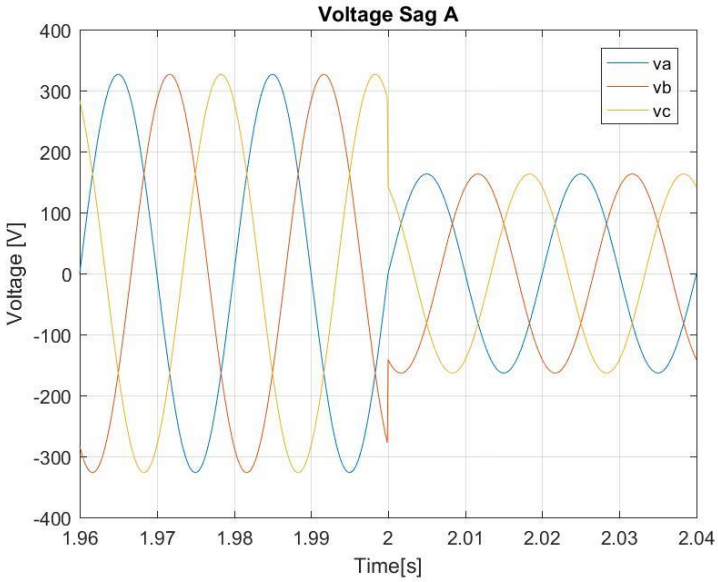


Figure 3.1 Voltage sag A test around t=2s

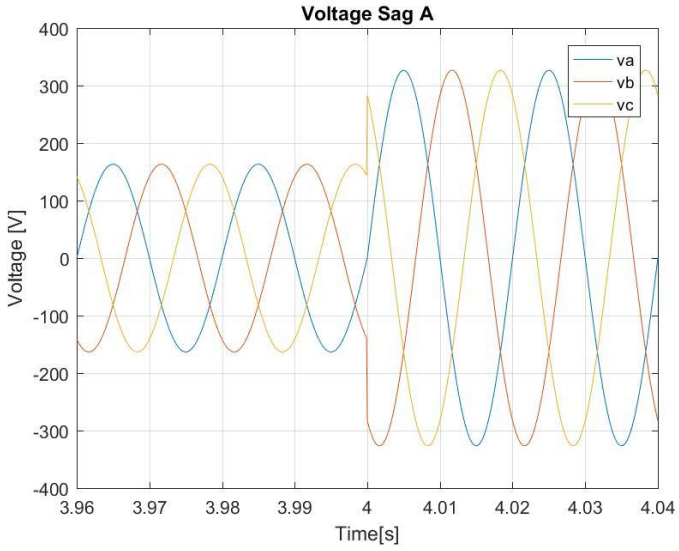


Figure 3.2 Voltage sag A test around t=4s

3.2. Voltage sag test B

$$V_{ABC} = \begin{bmatrix} 115\angle 0º \\ 230\angle -120º \\ 230\angle 120º \end{bmatrix}$$

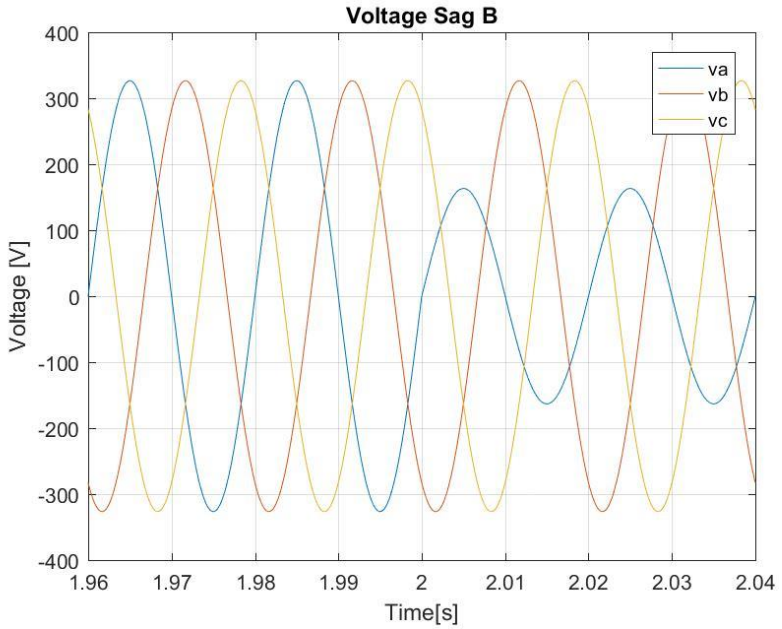


Figure 3.3 Voltage sag B test around t=2s

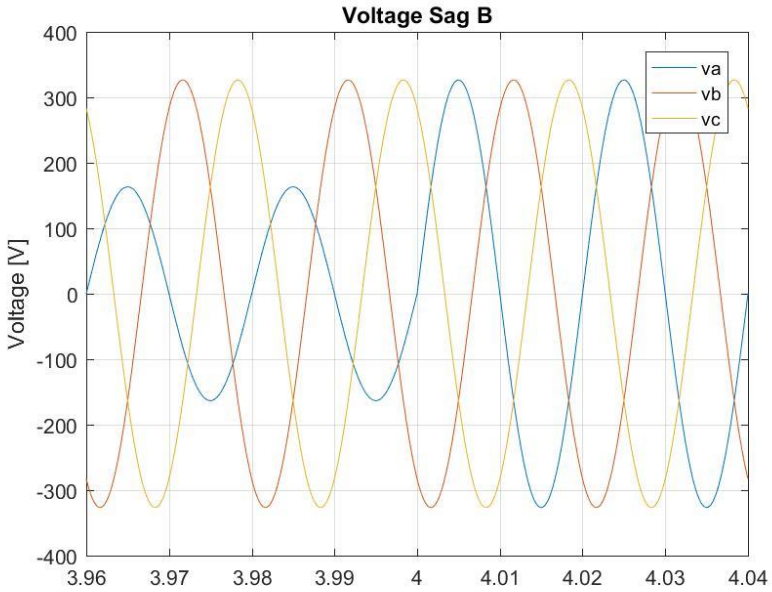


Figure 3.4 Voltage sag B test around t=4s

3.3 Voltage sag test C

$$V_{ABC} = \begin{bmatrix} 230\angle 0º \\ 151.8\angle -139º \\ 151.8\angle 139º \end{bmatrix}$$

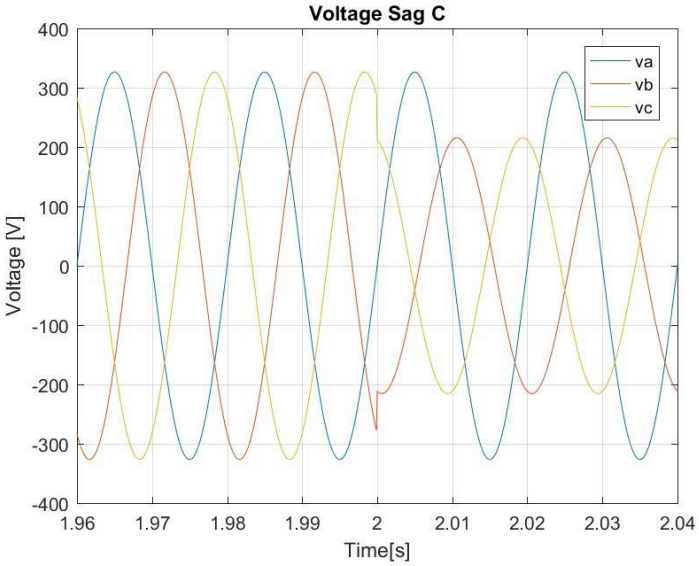


Figure 3.5 Voltage sag C test around t=2s

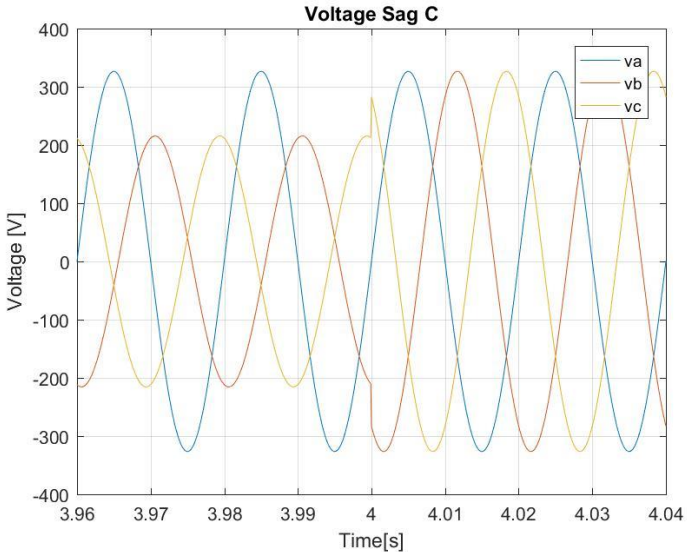


Figure 3.6 Voltage Sag C test around t=4s

3.4. Voltage sag test D

$$V_{ABC} = \begin{bmatrix} 115\angle 0º \\ 207.23\angle -106.1º \\ 207.23\angle 106.1º \end{bmatrix}$$

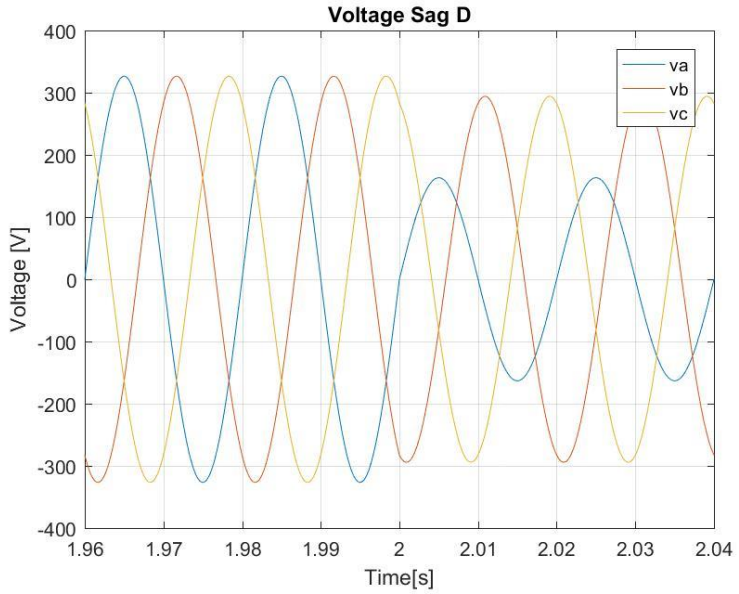


Figure 3.7 Voltage sag type D test around t=2s

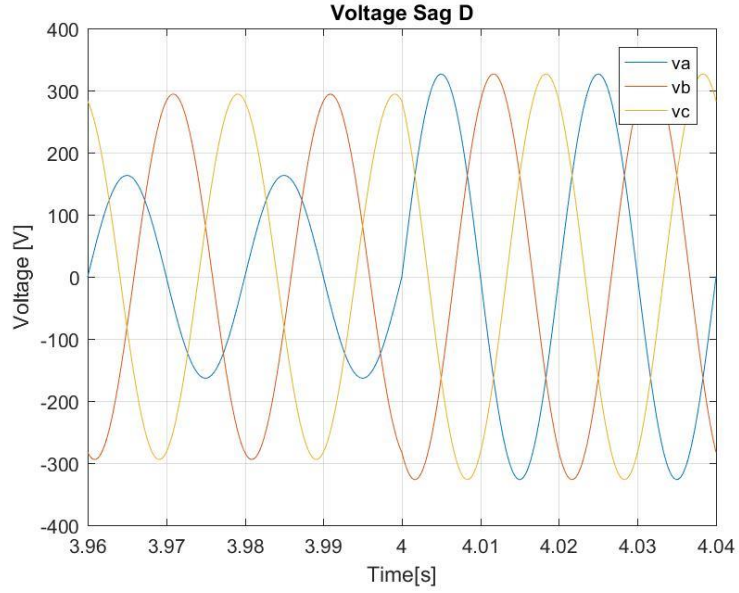


Figure 3.8 Voltage sag Type D around t=4s

3.5. Voltage sag test E

$$V_{ABC} = \begin{bmatrix} 230\angle 0º \\ 115\angle -120º \\ 115\angle 120º \end{bmatrix}$$

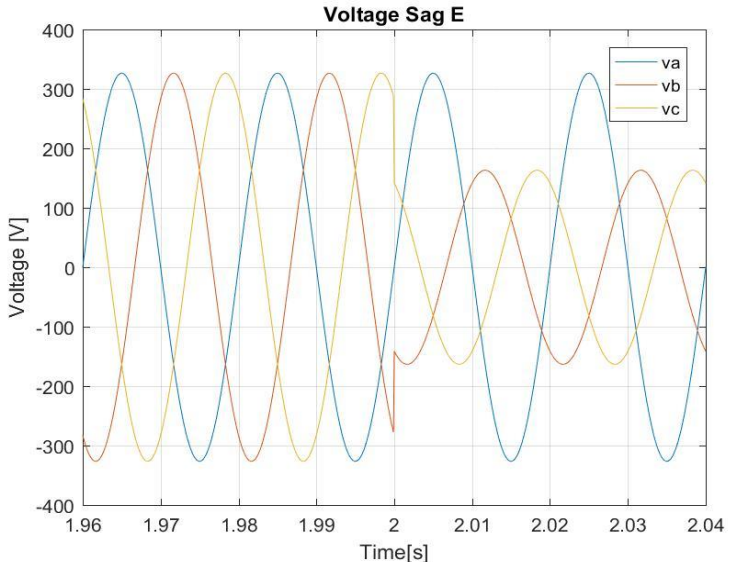


Figure 3.9 Voltage sag type E test around t=2s

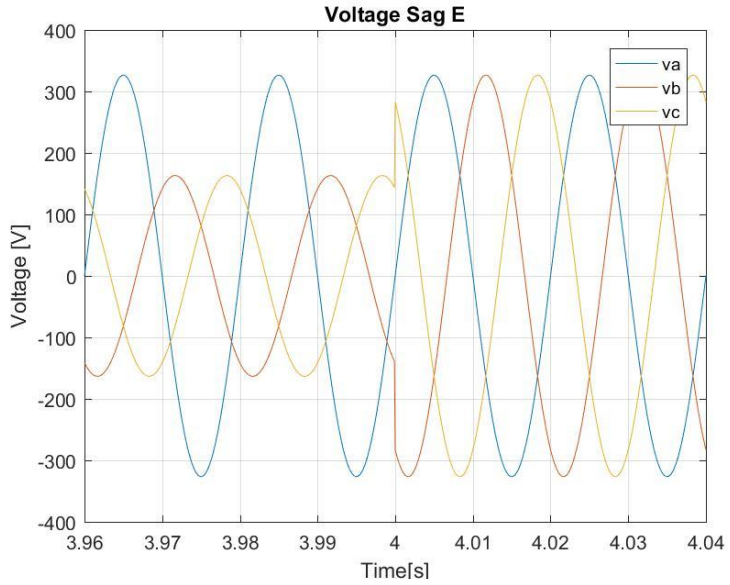


Figure 3.10 Voltage sag type E test around t=4s

3.6. Voltage sag test F

$$V_{ABC} = \begin{bmatrix} 115\angle 0º \\ 174.8\angle -109º \\ 174.8\angle 109º \end{bmatrix}$$

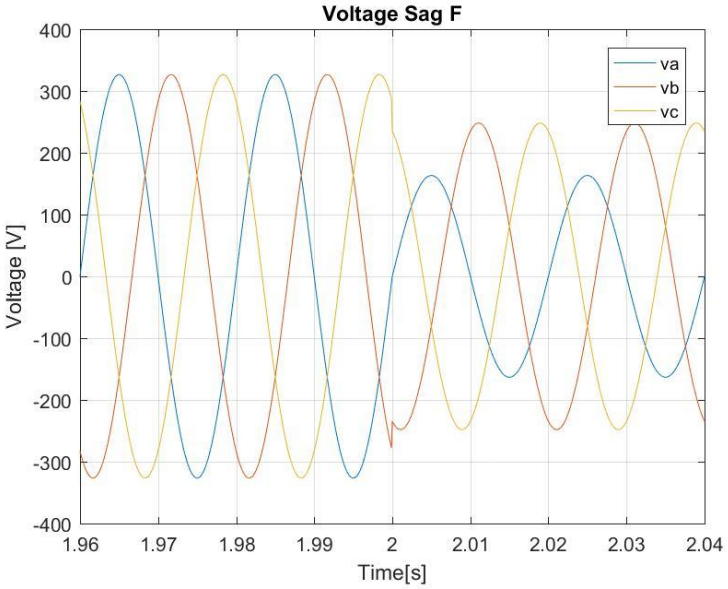


Figure 3.11 Voltage sag F test around t=2s

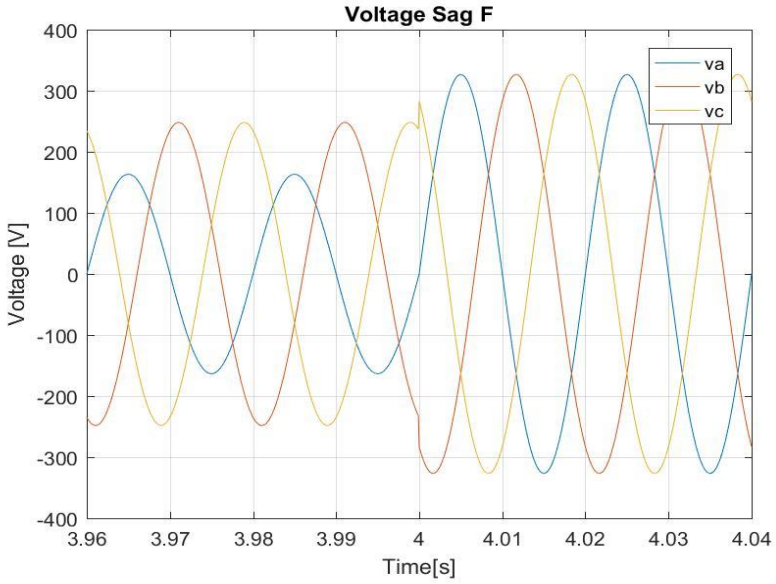


Figure 3.12 Voltage sag F test around t=4s

3.7. Voltage sag test G

$$V_{ABC} = \begin{bmatrix} 191.59\angle 0º \\ 138\angle -133.9º \\ 138\angle 133.9º \end{bmatrix}$$

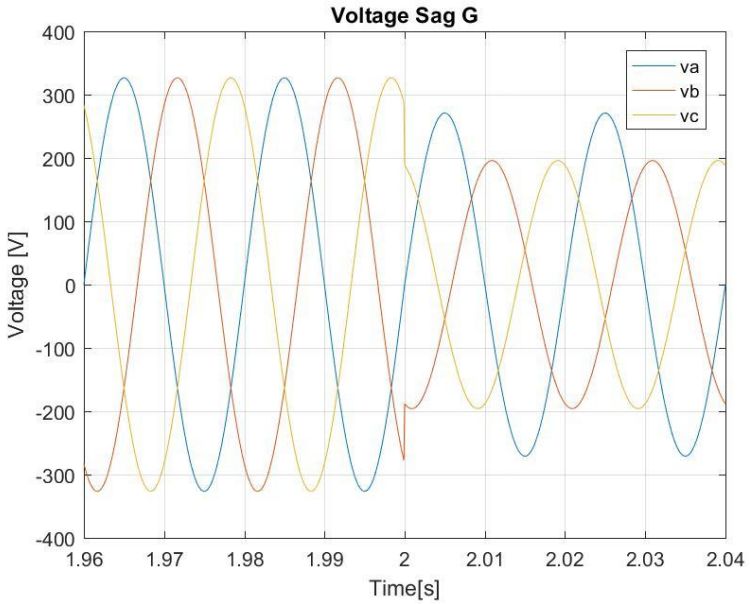


Figure 3.13 Voltage sag type G test around t=2s

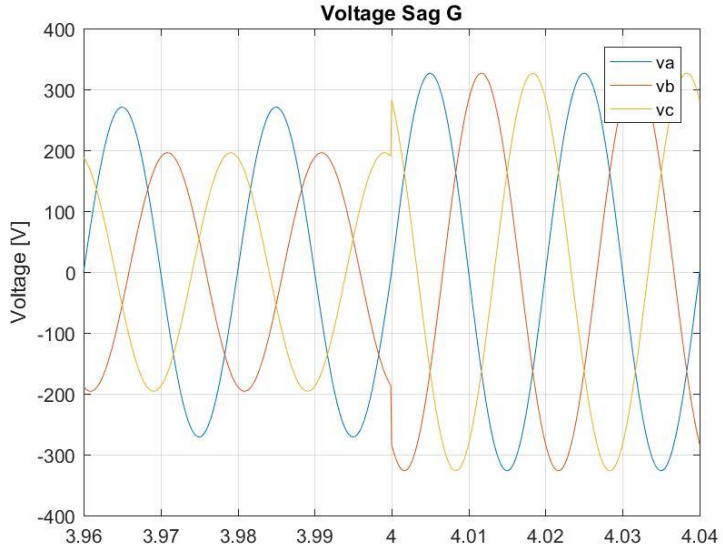


Figure 3.14 Voltage sag type G test around t=4s

3.8. Phase Jump Test

Upon defining the voltage sag tests, the following describes the input from t=2s to t=4s of the 90º phase jump test:

$$V_{ABC} = \begin{bmatrix} 230\angle 90º \\ 230\angle -30º \\ 230\angle 210º \end{bmatrix}$$

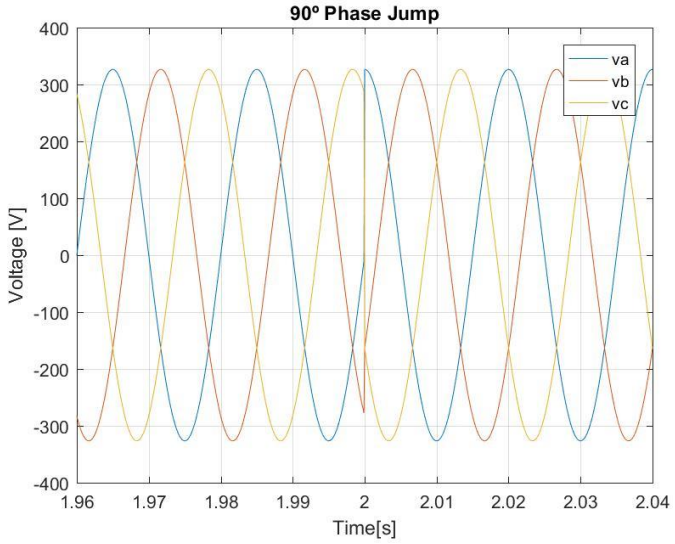


Figure 3.15 Phase Jump test around t=2s

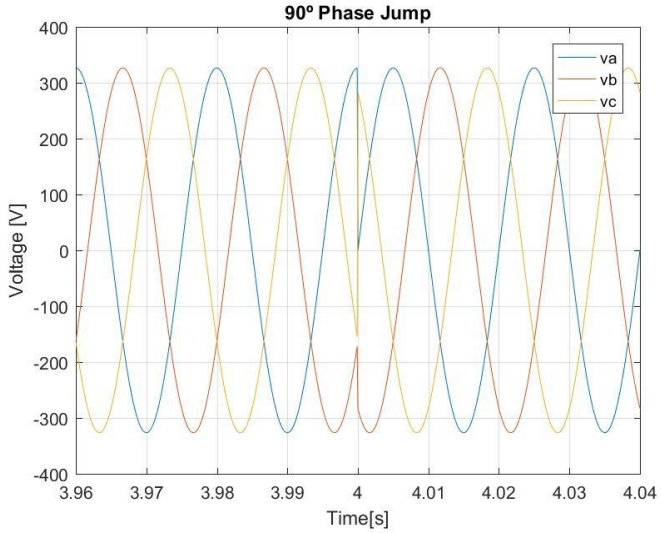


Figure 3.16 Phase jump test around t=4s

3.9. Frequency jump tests

The next two tests maintain the amplitude and waveform of the input voltage signal, but modify its frequency. The chosen frequency variation values are those defined in the frequency considerations chapter as the average yearly limits of a distribution network. When defining voltage vectors with a frequency different from the usual 50 Hz, phasors are not practical. Hence the sinusoidal definition of the input voltage vector.

+2Hz

$$V_{ABC} = \begin{bmatrix} 230\cos(52 \cdot 2\pi \cdot t - \frac{\pi}{2}) \\ 230\cos(52t \cdot 2\pi \cdot t - \frac{7\pi}{6}) \\ 230\cos(52t \cdot 2\pi \cdot t + \frac{\pi}{6}) \end{bmatrix}$$

-3Hz

$$V_{ABC} = \begin{bmatrix} 230\cos(47 \cdot 2\pi \cdot t - \frac{\pi}{2}) \\ 230\cos(47 \cdot 2\pi \cdot t - \frac{7\pi}{6}) \\ 230\cos(47 \cdot 2\pi \cdot t + \frac{\pi}{6}) \end{bmatrix}$$

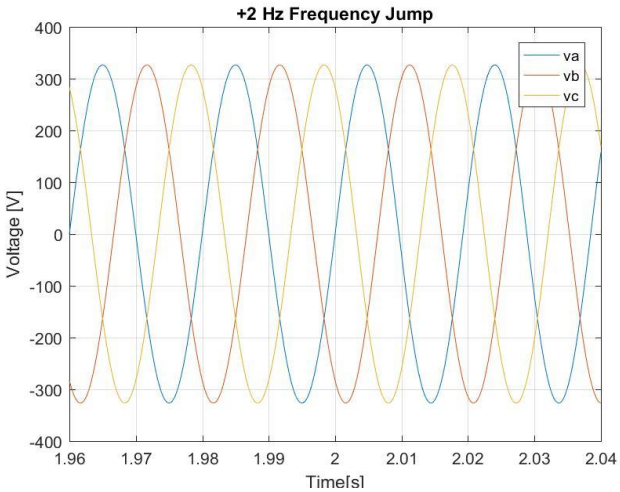


Figure 3.17 Frequency Jump test around t=2s

In order to

study the effect of voltage harmonics on the performance of the different PLLs,

three harmonic tests have been designed.

- Harmonic Test 1 focuses on odd non-homopolar harmonics (5^{th},7^{th},11^{th}).
- Harmonic Test 2 focuses on homopolar harmonics (3^{rd} and 9^{th}).
- Harmonic Test 3 combines both previous tests.

The amplitudes for every specific frequency was extracted from the total harmonic distortion limits table in the introduction chapter.

3.10.Harmonic test 1

$$V_{ABC} = \begin{bmatrix} 230\cos(50t - \frac{\pi}{2}) \\ 230\cos(50t - \frac{7\pi}{6}) \\ 230\cos(50t + \frac{\pi}{6}) \end{bmatrix} + \begin{bmatrix} 0.06 \cdot 230\cos(5 \cdot 50t - \frac{\pi}{2}) \\ 0.06 \cdot 230\cos(5 \cdot 50t - \frac{7\pi}{6}) \\ 0.06 \cdot 230\cos(5 \cdot 50t + \frac{\pi}{6}) \end{bmatrix}$$
$$+ \begin{bmatrix} 0.05 \cdot 230\cos(7 \cdot 50t - \frac{\pi}{2}) \\ 0.05 \cdot 230\cos(7 \cdot 50t - \frac{7\pi}{6}) \\ 0.05 \cdot 230\cos(7 \cdot 50t + \frac{\pi}{6}) \end{bmatrix} + \begin{bmatrix} 0.035 \cdot 230\cos(11 \cdot 50t - \frac{\pi}{2}) \\ 0.035 \cdot 230\cos(11 \cdot 50t - \frac{7\pi}{6}) \\ 0.035 \cdot 230\cos(11 \cdot 50t + \frac{\pi}{6}) \end{bmatrix}$$

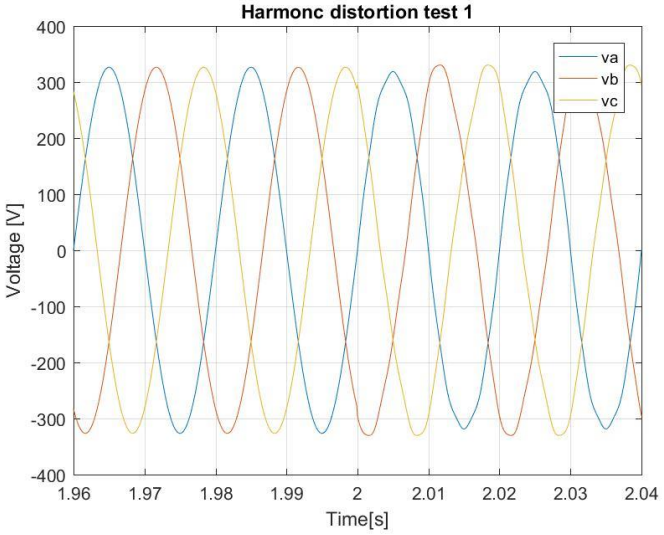


Figure 3.18 Harmonic Test 1 around t=2s

3.11.Harmonic Test 2

$$V_{ABC} = \begin{bmatrix} 230\cos(50t - \frac{\pi}{2}) \\ 230\cos(50t - \frac{7\pi}{6}) \\ 230\cos(50t + \frac{\pi}{6}) \end{bmatrix} + \begin{bmatrix} 0.05 \cdot 230\cos(3 \cdot 50t - \frac{\pi}{2}) \\ 0.05 \cdot 230\cos(3 \cdot 50t - \frac{7\pi}{6}) \\ 0.05 \cdot 230\cos(3 \cdot 50t + \frac{\pi}{6}) \end{bmatrix}$$
$$+ \begin{bmatrix} 0.015 \cdot 230\cos(9 \cdot 50t - \frac{\pi}{2}) \\ 0.015 \cdot 230\cos(9 \cdot 50t - \frac{7\pi}{6}) \\ 0.015 \cdot 230\cos(9 \cdot 50t + \frac{\pi}{6}) \end{bmatrix}$$

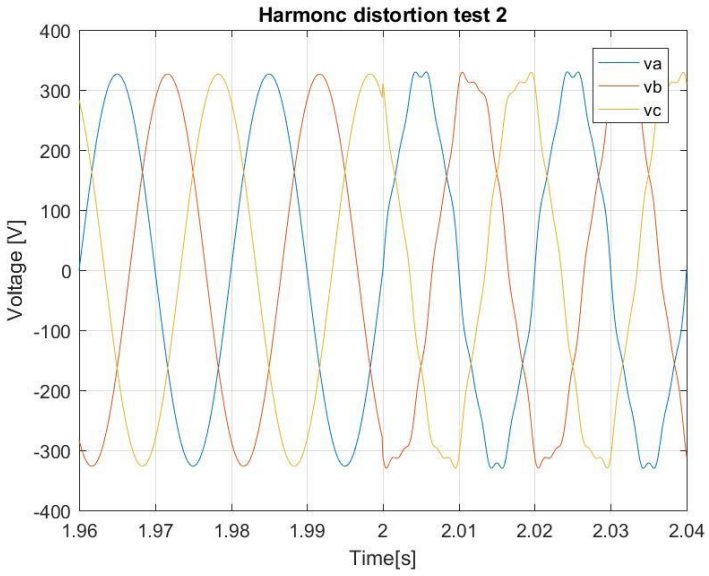


Figure 3.19 Harmonic test 2 around t=2s

3.12.Harmonic test 3

$$V_{ABC} = \begin{bmatrix} 230\cos(50t - \frac{\pi}{2}) \\ 230\cos(50t - \frac{7\pi}{6}) \\ 230\cos(50t + \frac{\pi}{6}) \end{bmatrix} + \begin{bmatrix} 0.05 \cdot 230\cos(3 \cdot 50t - \frac{\pi}{2}) \\ 0.05 \cdot 230\cos(3 \cdot 50t - \frac{7\pi}{6}) \\ 0.05 \cdot 230\cos(3 \cdot 50t + \frac{\pi}{6}) \end{bmatrix} +$$

$$\begin{bmatrix} 0.06 \cdot 230\cos(5 \cdot 50t - \frac{\pi}{2}) \\ 0.06 \cdot 230\cos(5 \cdot 50t - \frac{7\pi}{6}) \\ 0.06 \cdot 230\cos(5 \cdot 50t + \frac{\pi}{6}) \end{bmatrix} + \begin{bmatrix} 0.05 \cdot 230\cos(7 \cdot 50t - \frac{\pi}{2}) \\ 0.05 \cdot 230\cos(7 \cdot 50t - \frac{7\pi}{6}) \\ 0.05 \cdot 230\cos(7 \cdot 50t + \frac{\pi}{6}) \end{bmatrix}$$

$$+ \begin{bmatrix} 0.015 \cdot 230\cos(9 \cdot 50t - \frac{\pi}{2}) \\ 0.015 \cdot 230\cos(9 \cdot 50t - \frac{7\pi}{6}) \\ 0.015 \cdot 230\cos(9 \cdot 50t + \frac{\pi}{6}) \end{bmatrix} + \begin{bmatrix} 0.035 \cdot 230\cos(11 \cdot 50t - \frac{\pi}{2}) \\ 0.035 \cdot 230\cos(11 \cdot 50t - \frac{7\pi}{6}) \\ 0.035 \cdot 230\cos(11 \cdot 50t + \frac{\pi}{6}) \end{bmatrix}$$

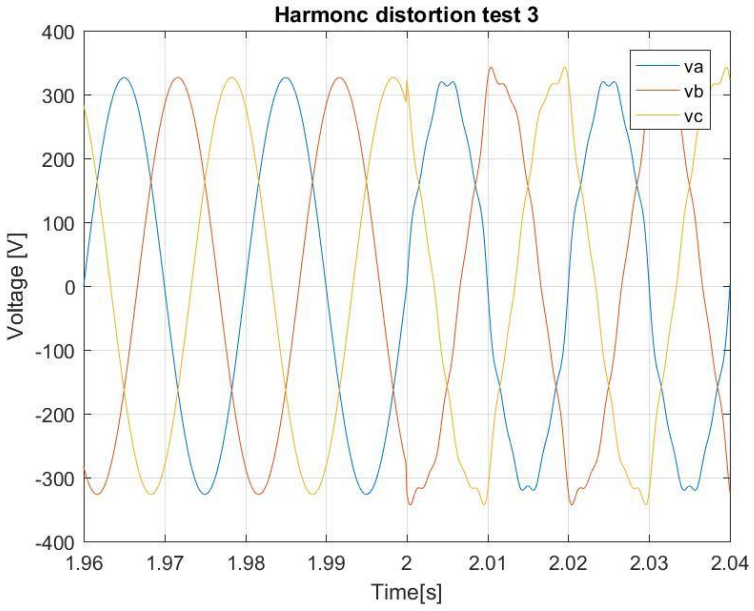


Figure 3.20 Harmonic test 3 around t=2s

All thirteen tests were implemented in the Matlab Simulink environment. In order to reproduce all of these faults, a block developed by the CITCEA team was used as a starting point. Certain changes were implemented since the initial block only enabled the output of three-phase voltage signals with harmonics 3, 5, 7, 9 and 11. These changes included the use of step inputs that modified the signal in t=2s and t=4s as well. The way in which the initial angle of every phase was introduced was also modified, making them an input variable and not a constant. Finally, an angular position reference was also introduced into the system as an output enabling the comparison of the PLL angle output with the actual angular position of the input signal.

3.13. Studied Variables

Upon simulating the voltage inputs and PLLs, the simulation results were studied in order to conduct the dynamic performance comparison. A few qualitative aspects were taken into account and were used as criteria to discard certain PLL designs that were initially selected for this study. These qualitative aspects included general stability of the simulation, how up to par the performance was compared to other PLL designs and the capacity of the PLL to recover normal functionality after the input signal returned to balanced status.

The main values used to compare dynamic performance of the PLLs under faults were the frequency output signal and the phase output signals [14].

Naturally, within these signals, 3 transient and 3 stationary behaviours were analysed. The three transient states correspond to:

- PLL initialization: Most of the studied PLL designs do not actually start outputting the exact phase of the input voltage signal. A fairly short transient state occurs during the locking process where the controller and filters enable correct tracking of the input phase.

- Fault occurrence: At t=2s, the input signal changes and therefore the PLL takes a short amount of time to adapt to the new input signal. Depending on the nature of this change, some of the designs will not succeed in tracking the correct phase of the input and will have an

oscillating error. In any case, whether or not the phase difference between the reference phase and the output phase oscillates, the PLL will require a certain amount of time to either stabilise the phase difference at 0, or to stabilise the amplitude of the phase difference oscillation.

- Return to normal functionality: At t=4, the input voltage signal will return to its balanced three-phase form. In this process and depending on the output of the PLL during the 2s fault duration, the control loop will take time to lock onto the input phase again. In this project, PLL designs that were not capable of returning to correct functionality were not included in the final version.

As explained in the introduction, one of the main scopes of this project is to provide a PLL reference guide for future CITCEA simulations and since the occurrence of faults is somewhat random and depends on mainly uncontrollable factors, PLLs that will cease to work upon regaining normality of the distribution network performance are not considered relevant.

In order to directly compare the output signals of the six studied PLLs, the following parameters were selected [15]:

- Peak Frequency Error: All of the PLL designs included in this study integrate the frequency to output the phase. Therefore, the frequency overshoots that occur during the previously mentioned transient states could essentially disrupt the stability of control loops that make use of the frequency. It is important to clarify that PLLs are usually used as part of a bigger control loop hence making a smooth output essential to successfully controlling an electric application.

- Peak Phase Error: As with the analysis of the frequency signal, the phase difference between the reference and the PLL's estimation also peaks coinciding with the voltage input variations. Studying this variable gives an insight as to how instantaneously inaccurate the PLL will be at the critical time mark, i.e. during the transient behaviour.

- Settling time: This variable is associated to the length of the transient behaviour of the PLL. Since the most relevant variable in this project is essentially the error between the PLL output phase and the actual phase of the voltage input, the settling time will be associated to this

variable. The regular definition of settling time is the time a variable takes to reach a value within 2% or 5% of its final value. Under proper functioning of the PLL, the phase difference will always converge to 0. Therefore, the chosen phase difference value to determine the settling time was 0.002 rad. 0.002 is approximately 0.1 degrees. Considering that a 0.1-degree angle difference produces differences of less than 0.5% in the calculation of sines and cosines, it was considered to be an appropriate approximation to be within 2% of 0. In the cases where the angle difference value oscillated at 100Hz between 2 values, the final amplitude of the oscillation was taken as final value and the settling time was calculated as the time at which the angle difference reached within 5% of that final value.

The studied parameters are essential in understanding how well a PLL adapts to changes in the input signal [8]. In the results section, these values will be paired up to the graphical representation of the output signals and explained in detail.

However, these values do not only depend on the nature of the input signal and the architecture of the PLL, they are also related to the tuning of the controllers within the PLL. The tuning of a PLL is directly related to the requirements of the rest of the control loops that make use of the frequency and phase outputs. Therefore, studying the tuning of a PLL in a project where no other control loops are included can be somewhat misleading. Hence, the values for the controller values have been extracted from a series of references from the literature. Summarising, since the tuning of a PLL within its stability limits involves a trade-off between the overshoot of both frequency and phase difference, and the settling time, each PLL should be retuned for specific applications.

4. Results

The following tables show the results and values extracted from the 13 voltage input tests. Bellow, each test and its results will be explained in more depth. For the sake of synthesis, the graphs attempt to illustrate multiple PLL results around both the t=2s and the t=4s time marks. Tables 4.1-4.2 Show the results filtering by PLL design:

	Sag A	Sag B	Sag C	Sag D	Sag E	Sag F	Sag G
DDsrf-PLL							
Peak Phase Error [º]	25.6268173	12.3949374	7.23437447	20.6108587	2.37E+01	20.4866882	11.41112742
Peak Frequency Error [Hz]	53.2849724	19.3487229	9.25E+00	4.73E+01	0.28663807	46.0740252	17.23134172
Settling time 1 [ms]	7	53	49	63	57	64	54
Settling time 2 [ms]	4	27	39	48	46	48	44
Phase oscillation during Fault [Hz]	0	0	0	0	0	0	0
Chung1-PLL							
Peak Phase Error [º]	5.0612E-08	11.4812888	0.09228475	19.4694005	3.46E+01	14.4381398	0.057265208
Peak Frequency Error [Hz]	1.2901E-08	25.8758805	1.69E-01	5.12E+01	0.25241578	33.2097088	0.15657124
Settling time 1 [ms]	<1	<1	<1	<1	<1	<1	<1
Settling time 2 [ms]	<1	<1	<1	<1	<1	<1	<1
Phase oscillation during Fault [Hz]	0	100	100	100	100	100	100
DSOGI-PLL							
Peak Phase Error [º]	6.91428035	4.00007083	2.74378991	6.28338072	2.12E+00	6.25079938	3.965355467
Peak Frequency Error [Hz]	3.48632915	2.63294257	1.52E+00	4.06E+00	0.04657501	3.69368669	2.123752951
Settling time 1 [ms]	57	24	27	25	29	27	28
Settling time 2 [ms]	26	23	25	24	27	25	26
Phase oscillation during Fault [Hz]	0	0	0	0	0	0	0
AB-PLL							
Peak Phase Error [º]	5.0651E-08	2.94841267	0.02446057	4.97352949	4.12E+00	3.69514312	0.015173507
Peak Frequency Error [Hz]	1.409E-10	3.52226661	2.88E-02	5.85E+00	0.0627437	4.39951114	0.017885039
Settling time 1 [ms]	0	34	34	39	27	33	36
Settling time 2 [ms]	0	27	<1	34	30	29	<1
Phase oscillation during Fault [Hz]	0.00E+00	1.00E+02	100	100	100	100	100
CHUNG2-PLL							
Peak Phase Error [º]	5.0899E-08	11.3475484	0.09563982	18.7862187	2.95E+01	13.6994699	0.058481428
Peak Frequency Error [Hz]	3.1599E-09	22.9115837	1.61E-01	4.31E+01	0.24158254	29.4136816	0.141887243
Settling time 1 [ms]	<1	<1	<1	<1	<1	<1	<1
Settling time 2 [ms]	<1	<1	<1	<1	<1	<1	<1
Phase oscillation during Fault [Hz]	0	100	100	100	100	100	100
DAB-PLL							
Peak Phase Error [º]	4.62789905	2.62276418	1.814457	4.10648942	1.71E+00	4.00465195	2.627808122
Peak Frequency Error [Hz]	2.55790417	1.89193068	1.07E+00	2.88E+00	0.03168682	2.6487895	1.523827546
Settling time 1 [ms]	50	38	39	43	39	46	48
Settling time 2 [ms]	46	38	38	43	37	45	41
Phase oscillation during Fault [Hz]	0	0	0	0	0	0	0

Table 4.1 Simulation results for the studied PLLs in the voltage sag tests

As can be seen, the results of the Voltage sag tests do not differ greatly. This is mainly because aside from the A type voltage sag, all of the other tests introduce

a negative sequence component during the fault. Upon occurrence of this phenomenon, the PLLs that do not differentiate between positive and negative sequence output a 100 Hz oscillating value for both frequency and Phase. The input voltage signals for most of these tests are vaguely similar and mainly rely on amplitude variations and small phase shifts of the B and C phases. For this reason, the differences between the performance of the various PLLs is fairly consistent between all tests.

	Phase Jump	"+2Hz Jump"	"-3Hz Jump"	Harmonics 1	Harmonics 2	Harmonics3
DDsrf-PLL						
Peak Phase Error [º]	90.0000001	0.0220762	0.03347906	6.07200929	6.74235015	11.8592831
Peak Frequency Error [Hz]	6442.44748	2.00681417	3.0103401	16.4501204	39.7167195	59.0131393
Settling time 1 [ms]	18	<1	<1			
Settling time 2 [ms]	7	<1	<1	36	39	41
Chung1-PLL						
Peak Phase Error [º]	90.0000001	0.01636403	0.02454604	3.58085171	6.29044416	8.26107989
Peak Frequency Error [Hz]	7002.66031	2.00000267	3.00000398	10.3228086	38.8230953	46.1390103
Settling time 1 [ms]	<1	<1	<1			
Settling time 2 [ms]	<1	<1	<1	1	1	1
DSOGI-PLL						
Peak Phase Error [º]	90.0000062	4.40587133	6.65966044	0.97940826	0.73757782	1.35206885
Peak Frequency Error [Hz]	31.9705092	2.09745546	3.12182526	1.08989704	1.34284923	2.01244993
Settling time 1 [ms]	130	134	109			
Settling time 2 [ms]	133	87	100	14	16	16
AB-PLL						
Peak Phase Error [º]	90.000013	7.06286855	10.6283408	0.76176829	0.68950622	1.04419576
Peak Frequency Error [Hz]	16.2656352	2.00000029	3.00000044	1.09587163	1.79840378	2.38190284
Settling time 1 [ms]	68	23	35			
Settling time 2 [ms]	70	41	45	15	15	21
CHUNG2-PLL						
Peak Phase Error [º]	90	0.28781528	0.43173019	3.07491449	5.47878923	6.97338817
Peak Frequency Error [Hz]	350.133015	2.07310766	3.10966671	7.3310725	24.2243462	31.448499
Settling time 1 [ms]	36	11	<1			
Settling time 2 [ms]	36	10	15	2	1	2
DAB-PLL						
Peak Phase Error [º]	90.0000184	7.69078103	11.5802428	0.6980496	0.58211995	0.92664302
Peak Frequency Error [Hz]	14.2125677	2.00000041	3.00000063	0.97166883	1.62992515	2.13584311
Settling time 1 [ms]	75	23	43			
Settling time 2 [ms]	80	47	54	16	14	22

Table 4.2 Phase jump and Frequency alteration test results for the studied PLLs

In contrast with the voltage sag tests, performance consistency of the different PLL designs throughout the tests is compromised by the major differences in the voltage inputs. The first three tests do not introduce negative sequence components into the system and therefore no oscillation can be observed. However, the tests that included harmonics during the fault had a very big impact on the precision of the PLL's phase estimation. The harmonics produced massive interferences in the output signal that could not be controlled by any of the PLLs. Nevertheless, as commented in previous chapters of this project, all of the studied PLLs were capable of regaining precise phase estimation after the disturbance ended at t=4s.

4.1. Voltage sag test A

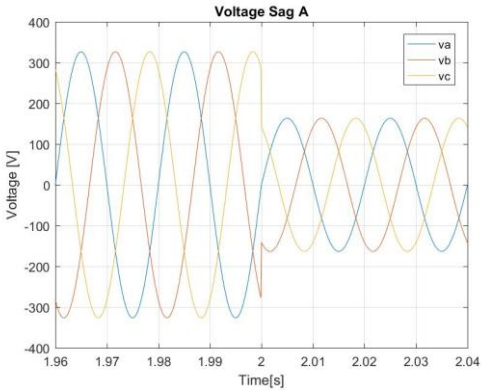


Figure 4.1 Voltage Sag A test

		DDSRF-PLL	SRF1-PLL	DSOGI-PLL	AB-PLL	SRF2-PLL	DAB-PLL
Voltage sag A	Peak Freq Error [Hz]	53.2849724	1.2901E-08	3.48632915	1.409E-10	3.1599E-09	2.55790417
	Peak Frequency Error [%]	106.569945	2.5802E-08	6.9726583	2.818E-10	6.31979E-09	5.11580834
	Peak Phase error [º]	25.6269159	5.0612E-08	6.91430696	5.0651E-08	5.08988E-08	4.62791686
	Ts transient 1 [ms]	70	<1	57	<1	<1	50
	Ts transient 2 [ms]	40	<1	26	<1	<1	46
	Peak Frequency error 1 [Hz]	53.2849724	1.2393E-08	3.48632915	1.409E-10	6.76302E-10	2.55790417
	Peak Frequency error 2 [Hz]	10.7809327	1.2901E-08	1.79650138	9.9497E-11	3.1599E-09	0.90521001
	Peak Phase error 1 [º]	25.6269159	25.6269159	25.6269159	25.6269159	25.6269159	25.6269159
	Peak Phase error 2 [º]	9.29431117	9.29431117	9.29431117	9.29431117	9.294311173	9.29431117

Table 4.3 Voltage sag A test results

Test results for an A type voltage sag show that the simpler PLL designs are much more efficient when tracking phase through amplitude variations of the three phases. So long as symmetry of and balance of the voltage input is maintained, this situation will persist. The really fast response time is mainly due to the lack of extra filters aside from the PI controller. Filters are capable of reducing the amplitude of oscillations at given frequencies, but also produce a delay of the output thus making the PLL slower. Since there is no negative sequence component in this input, simple is best.

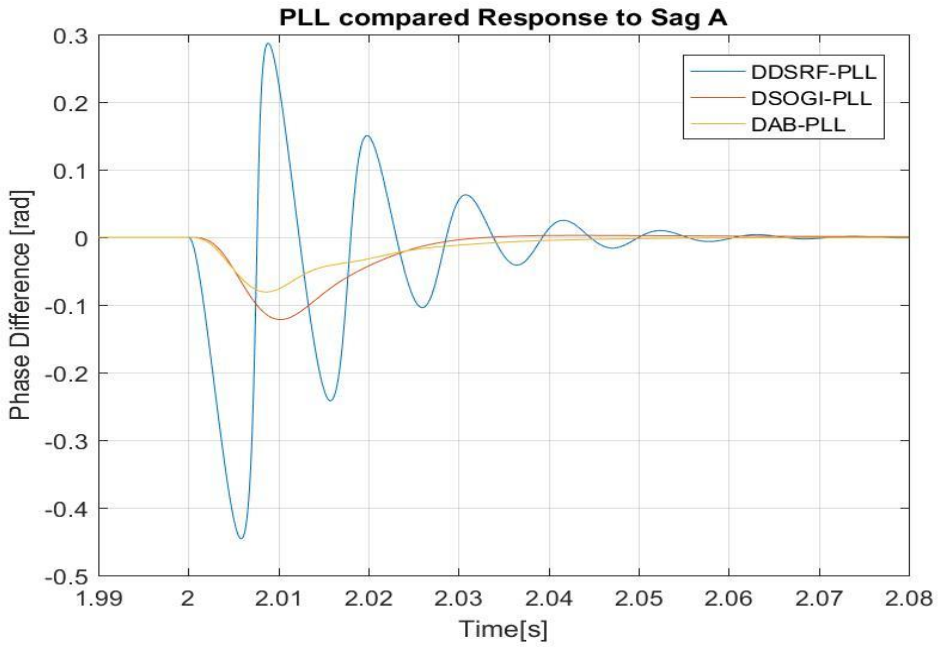


Figure 4.2 First transient behaviour for phase difference under Voltage sag A test (DSOGI, DAB and DDSRF)

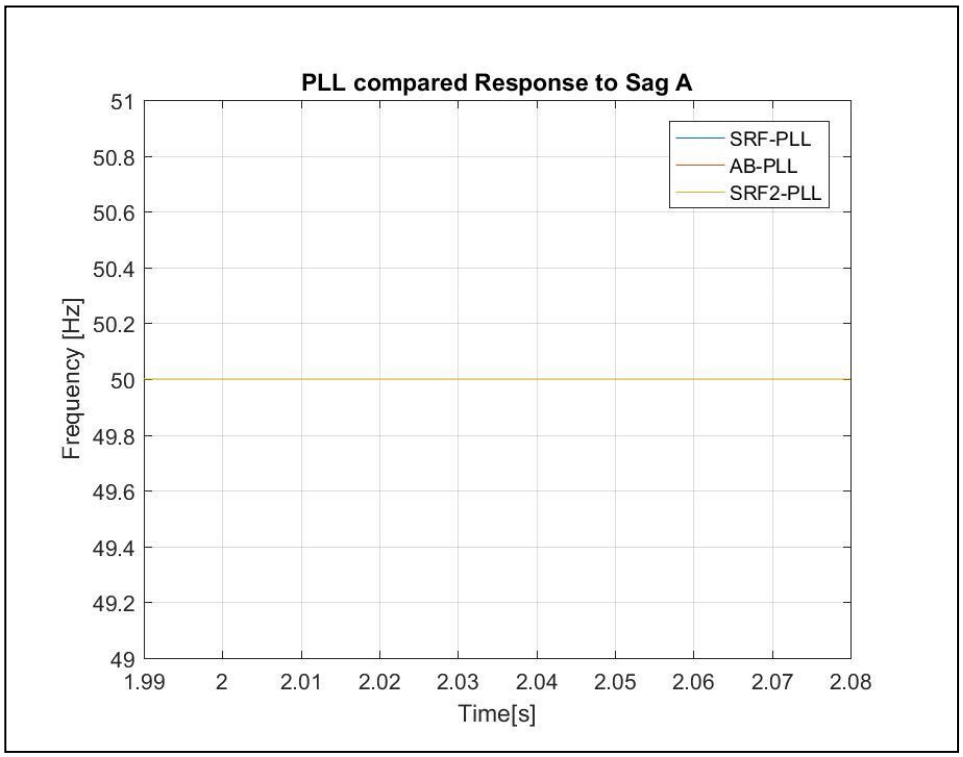


Figure 4.3 First transient behaviour for phase difference under Voltage sag A test (SRF1, SRF2 and AB)

The simpler PLLs directly use the positive sequence component and do not take into account the negative sequence. For example, the DDSRF PLL would have a completely non-oscillating signal through the positive park rotation, and a 100 Hz oscillation in the negative park rotation output which has to be filtered producing a delay and a fairly steep transient state, whereas the SRF-PLL directly does not notice that there has been a change in the voltage input. Regaining normal functioning, the situation looks exactly the same:

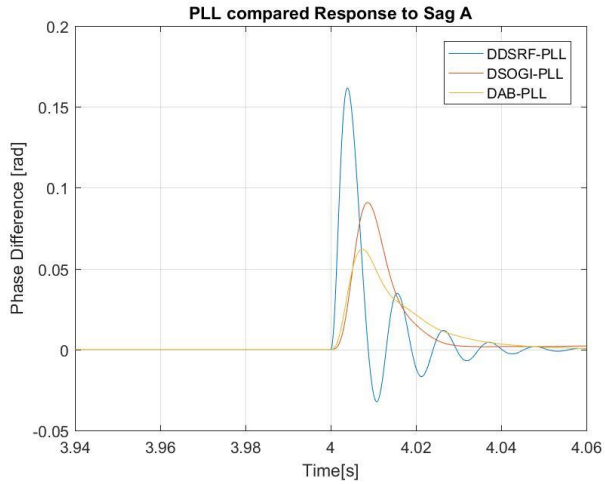


Figure 4.4 Second transient behaviour for Phase difference under Voltage sag A test (DSOGI, DDSRF and DAB)

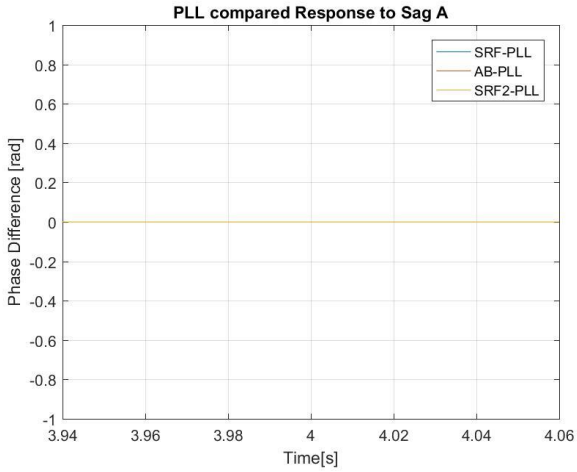


Figure 4.5 Second transient behaviour for phase difference under Voltage sag A (SRF1, SRF2 and AB)

Upon analysing the performance of the PLLs under the voltage sag A test, the most efficient in terms of frequency overshoot and settling time were the SRF and the AB designs.

4.2. Unbalanced voltage input tests

Table 4.4 shows the results for the unbalanced voltage sag tests:

		DDSRF-PLL	SRF1-PLL	DSOGI-PLL	AB-PLL	SRF2-PLL	DAB-PLL
Voltage sag B	Peak Freq Error [Hz]	19.3487229	25.87588053	2.632942566	3.522266613	22.9115837	1.891930681
	Peak Frequency Error [%]	38.6974459	51.75176106	5.265885132	7.044533226	45.8231675	3.783861362
	Peak Phase error [º]	12.3949851	11.48133297	4.000086218	2.948424013	11.3475921	2.622774277
	Ts transient 1 [ms]	53	<1	24	34	<1	38
	Ts transient 2 [ms]	27	<1	23	27	<1	38
	Peak Frequency error 1 [Hz]	19.3487229	25.87588053	2.632942566	3.522266613	22.9115837	1.891930681
	Peak Frequency error 2 [Hz]	14.5651094	16.66531696	1.64191796	3.020028622	16.7292684	0.96696929
	Peak Phase error 1 [º]	12.3949851	11.48133297	4.000086218	2.948424013	11.3475921	2.622774277
	Peak Phase error 2 [º]	9.98636735	11.48132759	3.797192546	1.910938888	11.3475895	2.618723484
Voltage sag C	Peak Freq Error [Hz]	9.25E+00	1.69E-01	1.52E+00	2.88E-02	1.61E-01	1.07E+00
	Peak Frequency Error [%]	1.85E+01	3.37E-01	3.04E+00	5.76E-02	3.23E-01	2.15E+00
	Peak Phase error [º]	7.23440231	0.092285102	2.743800465	0.024460668	0.09564019	1.814463982
	Ts transient 1 [ms]	49	<1	27	34	<1	39
	Ts transient 2 [ms]	39	<1	25	<1	<1	38
	Peak Frequency error 1 [Hz]	9.25E+00	1.69E-01	1.52E+00	2.88E-02	1.61E-01	1.07E+00
	Peak Frequency error 2 [Hz]	5.28E+00	1.68E-01	8.51E-01	2.67E-02	1.61E-01	4.26E-01
	Peak Phase error 1 [º]	7.23440231	0.092285102	2.743800465	0.024460668	0.09564019	1.814463982
	Peak Phase error 2 [º]	4.84408235	0.092285027	2.421048725	0.01528661	0.09513643	1.61993317
Voltage sag D	Peak Freq Error [Hz]	4.73E+01	5.12E+01	4.06E+00	5.85E+00	4.31E+01	2.88E+00
	Peak Frequency Error [%]	9.47E+01	1.02E+02	8.11E+00	1.17E+01	8.61E+01	5.76E+00
	Peak Phase error [º]	20.610938	19.46947545	6.283404897	4.973548625	18.786291	4.106505226
	Ts transient 1 [ms]	63	<1	25	39	<1	43
	Ts transient 2 [ms]	48	<1	24	34	<1	43
	Peak Frequency error 1 [Hz]	4.73E+01	5.12E+01	4.06E+00	5.85E+00	4.31E+01	2.88E+00
	Peak Frequency error 2 [Hz]	1.88E+01	2.50E+01	2.51E+00	5.11E+00	2.56E+01	1.48E+00
	Peak Phase error 1 [º]	20.610938	19.46947545	6.283404897	4.973548625	18.786291	4.075075643
	Peak Phase error 2 [º]	14.9820102	19.46832805	5.814503987	3.298945663	18.7862872	4.106505226
Voltage sag E	Peak Freq Error [Hz]	2.37E+01	3.46E+01	2.12E+00	4.12E+00	2.95E+01	1.71E+00
	Peak Frequency Error [%]	4.75E+01	6.93E+01	4.24E+00	8.24E+00	5.90E+01	3.42E+00
	Peak Phase error [º]	16.423215	14.46241469	2.668561903	3.594962889	13.8417131	1.815528282
	Ts transient 1 [ms]	57	<1	29	27	<1	39
	Ts transient 2 [ms]	46	<1	27	30	<1	37
	Peak Frequency error 1 [Hz]	2.37E+01	3.46E+01	2.12E+00	4.12E+00	2.95E+01	1.71E+00
	Peak Frequency error 2 [Hz]	1.19E+01	2.00E+01	1.07E+00	3.80E+00	1.99E+01	1.18E+00
	Peak Phase error 1 [º]	16.423215	14.46241403	2.668561903	3.594962889	13.8417131	1.815528282
	Peak Phase error 2 [º]	6.92760775	14.46241469	2.144613411	2.419961671	13.7236246	1.38323609
Voltage sag F	Peak Freq Error [Hz]	46.0740252	33.20970879	3.693686694	4.39951114	29.4136816	2.648789505
	Peak Frequency Error [%]	92.1480505	66.41941758	7.387373388	8.79902228	58.8273632	5.297579009
	Peak Phase error [º]	20.4867671	14.43819537	6.250823439	3.695157335	13.6995226	4.004667365
	Ts transient 1 [ms]	64	<1	27	33	<1	46
	Ts transient 2 [ms]	48	<1	25	29	<1	45
	Peak Frequency error 1 [Hz]	46.0740252	33.20970879	3.693686694	4.39951114	29.4136816	2.648789505
	Peak Frequency error 2 [Hz]	18.1774546	24.06970411	2.097049644	3.798068495	24.1389451	1.174344567
	Peak Phase error 1 [º]	20.4867671	14.43819537	6.250823439	3.695157335	13.6995226	4.004667365
	Peak Phase error 2 [º]	11.8354869	14.43819174	5.451852372	2.415956799	13.6931073	3.851875609
Voltage sag G	Peak Freq Error [Hz]	17.2313417	0.15657124	2.123752951	0.017885039	0.14188724	1.523827546
	Peak Frequency Error [%]	34.4626834	0.31314248	4.247505901	0.035770079	0.28377449	3.047655093
	Peak Phase error [º]	11.4111713	0.057265428	3.965370726	0.015173565	0.05848165	2.627818235
	Ts transient 1 [ms]	54	<1	28	36	<1	48
	Ts transient 2 [ms]	44	<1	26	<1	<1	41
	Peak Frequency error 1 [Hz]	17.2313417	0.104438711	2.123752951	0.017885039	0.0999464	1.523827546
	Peak Frequency error 2 [Hz]	7.1634157	0.15657124	1.167428737	0.016557382	0.14188724	0.584293332
	Peak Phase error 1 [º]	11.4111713	0.057265428	3.965370726	0.015173565	0.05848165	2.627818235
	Peak Phase error 2 [º]	6.4363752	0.057265131	3.303642162	0.009479605	0.05812006	2.242354807

Table 4.4 Results for Voltage sag test with unbalanced phasors

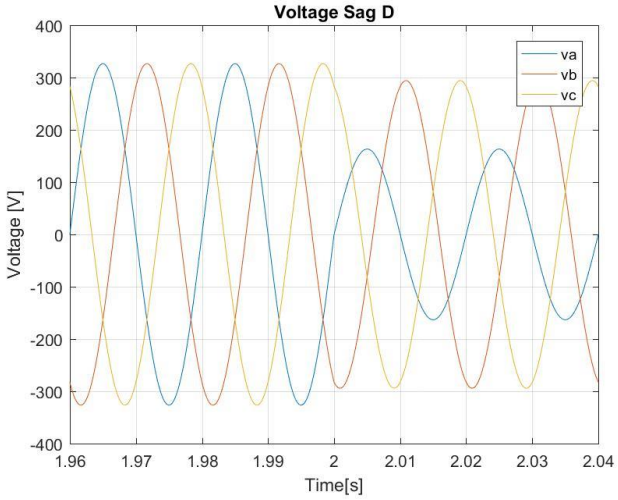


Figure 4.6 Unbalanced Voltage sag type D

Analysis of the voltage sag tests from sag B to sag G is very similar. In all of these tests, the negative sequence component introduced during the fault separated the PLLs into two groups. Those that were capable of locking onto the voltage input's phase during the fault and those that couldn't. For the sake of synthesis, the results will be analysed together

Figs 4.7-4.8 illustrate the dynamic response of the PLLs as they adapt to the input change.

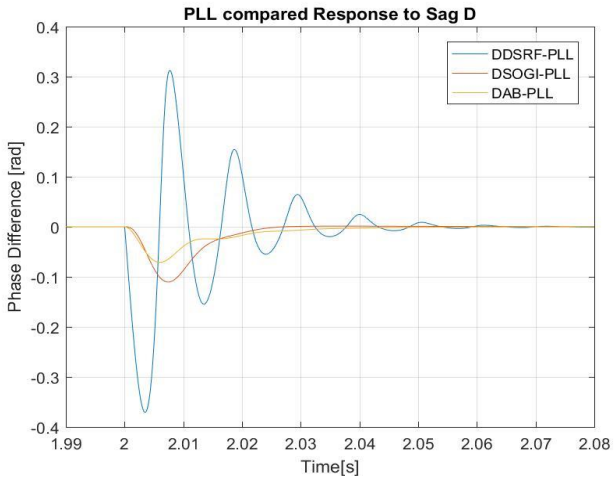


Figure 4.7 First transient behaviour for phase difference under unbalanced voltage sags (DSOGI, DDSRF and DAB)

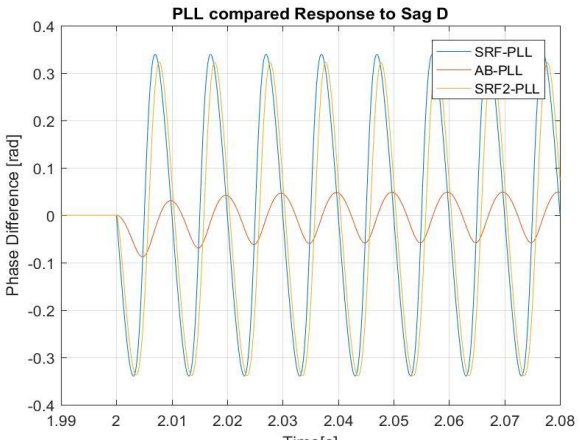


Figure 4.8 First transient behaviour for phase difference under unbalanced voltage sags (SRF1, SRF2 and AB)

The structures of the DDSRF-PLL, DSOGI-PLL and the DAB-PLL enable them to lock with the phase of the input signal. The DSOGI and DAB designs perform much better than the DDSRF as can be seen in the first figure. In contrast, the simpler PLL designs show a 100 Hz oscillation that corresponds to the interference the negative sequence component produces in the park rotation output.

In the studied voltage sags, the voltage input is a sum of a phasor set that rotates at 50 Hz and another phasor set that rotates at -50 Hz.

Naturally, if the park rotation turns at 50 Hz the negative sequence component will appear as a 100 Hz oscillation instead of the desired constants associated to the application of the transform.

Fig 4.8 shows the amplitude of the oscillations in the phase difference varies with each type of voltage sag:

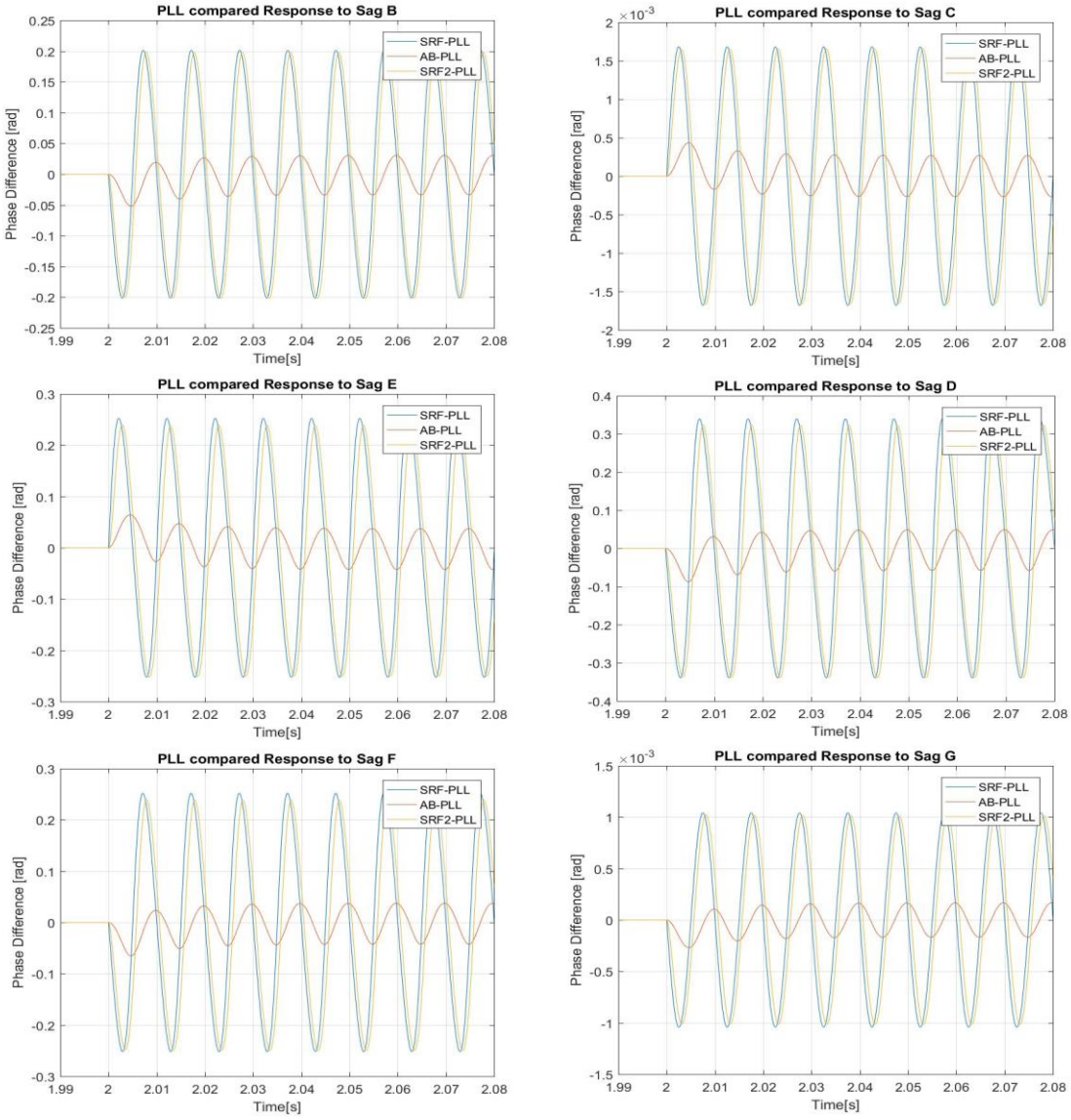


Figure 4.9 Phase Difference oscillations throughout the unbalanced voltage sag tests (SRF1, SRF2 and AB)

Studying the manner in which the angle estimation error behaves throughout all of these tests raises a very interesting point. As explained in the introductory chapter, most of the types of voltage sag occur as a consequence of propagation of other voltage sags through a circuit.

Table 4.5 shows the propagation of sags through Dy transformers:

Fault type	PCC1	PCC2	PCC3
Three-phase/three-phase to ground	A	A	A
Single-phase to ground	B	C	D
Two-phase	C	D	C
Two-phase to ground	E	F	G

Table 4.5 Voltage sag Propagation through a Dy transformer

If we analyse the data for peak phase error of the different sorts of voltage sags, one can come to terms with the fact that feeding the voltage from different points of common coupling into a PLL will have a direct impact on how precise the angle estimation will be during the same fault. Therefore, in specific cases like that of a voltage sag propagation throughout a Dy transformer, the PLLs will minimise the error during the fault if connected to the right PCC. This can be applied if the delay introduced on the voltage signal by the actual transformer is small enough.

So far, the results section has focused entirely on studying phase difference values between the PLL output and the reference. In all of the studied tests, the frequency values behave in a very similar fashion to the phase difference values. In all of the designs, the phase signal is equal to the frequency signal fed through an integrator. Since this chapter could be much longer than it currently is, the frequency values will be shown in the summary tables.

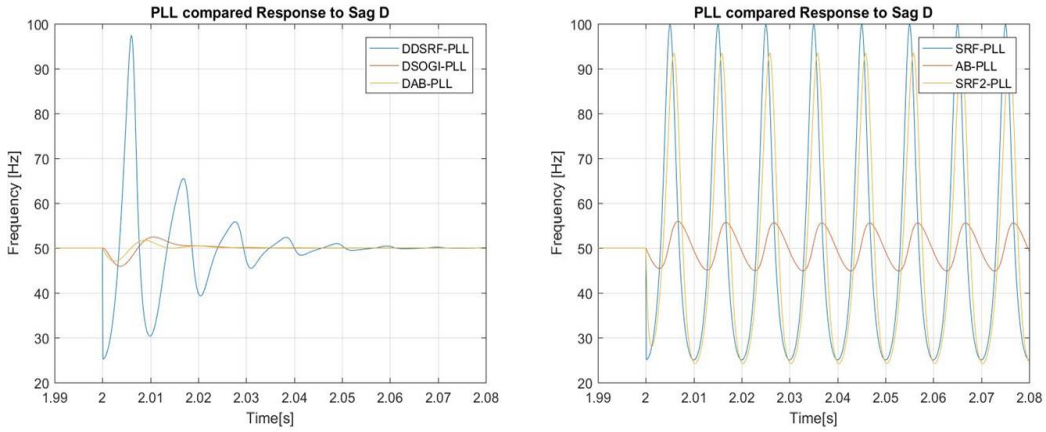


Figure 4.10 PLL Frequency transient behaviour for voltage sag D

Upon inspection of the results, due to the negative sequence component introduced by the unbalanced voltage sags, the PLLs that were capable of dealing with the disturbances and controlling the error were more successful. Therefore the DDSRF, DSOGI and DAB are clearly the recommended PLL choices for these scenarios due to their filtering capabilities.

4.3. Phase Jump

The phase jump test introduces a very steep change in the phase of the voltage input signal. The following results show the dynamic behaviour of the PLLs to a $\frac{\pi}{2}$ phase jump:

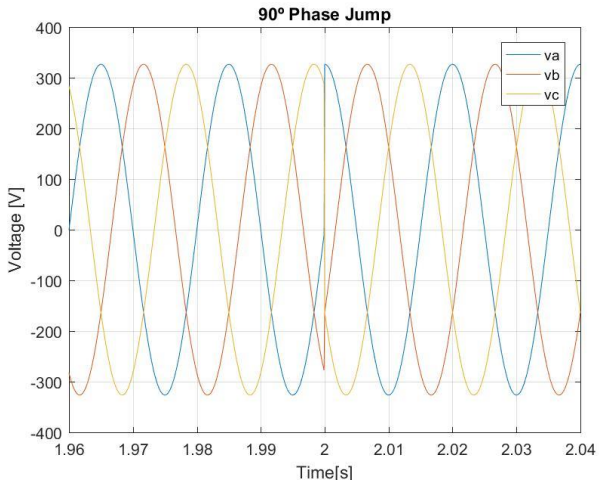


Figure 4.11 Phase jump test

Table 4.6 shows the results for the phase jump test:

		DDSRF-PLL	SRF1-PLL	DSOGI-PLL	AB-PLL	SRF2-PLL	DAB-PLL
Phase Jump	Peak Freq Error [Hz]	6442.447483	7002.66031	31.9705092	16.2656352	350.133015	14.2125677
	Peak Frequency Error [%]	12884.89497	14005.3206	63.9410184	32.5312704	700.266031	28.4251354
	Peak Phase error [º]	90.00034639	90.0003464	90.0003525	90.0003593	90.0003464	90.0003648
	Ts transient 1 [ms]	18	<1	130	68	36	75
	Ts transient 2 [ms]	7	<1	133	70	36	80
	Peak Frequency error 1 [Hz]	6442.447483	7002.66031	31.9705092	16.2656352	350.133015	14.2125677
	Peak Frequency error 2 [Hz]	6442.447482	7002.66031	26.202483	16.2656315	350.133015	12.5964946
	Peak Phase error 1 [º]	90.00034634	90.0003463	90.0003525	90.0003463	90.0003463	90.0003463
	Peak Phase error 2 [º]	90.00034639	90.0003464	90.0003522	90.0003593	90.0003464	90.0003648

Table 4.6 Phase jump test results

The dynamic performance of the PLLs under this type of fault is relatively similar. Surprisingly enough, the PLLs that performed best under unbalanced voltage inputs are not quite as efficient under this situation.

Settling time values for the more complex PLL designs tend to be higher than those of the simpler design. Since this type of voltage fault introduces a certain maximum phase error which is the same for all 6 PLLs, the speed of the controllers stands out over other qualities.

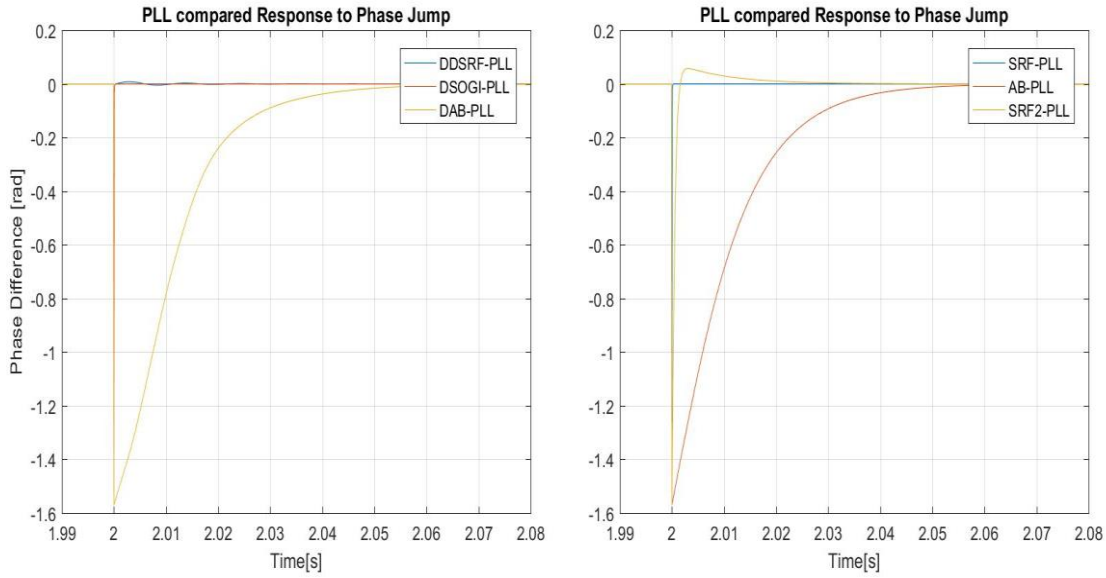


Figure 4.12 Phase difference values for the phase jump test

In this test, all PLLs show a massive increase in phase error at the time of the fault. Since the phase shift affects all phases at the same time, the symmetry of the system is maintained throughout the fault. Therefore, the PLLs only lose track

of the voltage input phase for a short time. Within two cycles all of the PLLs regain tracking capability. However, near the t=2s mark, the frequency overshoot is very different for the designs. Should the frequency be an important part of a larger control system, the choice of an adequate PLL should probably be based on minimising the frequency overshoot.

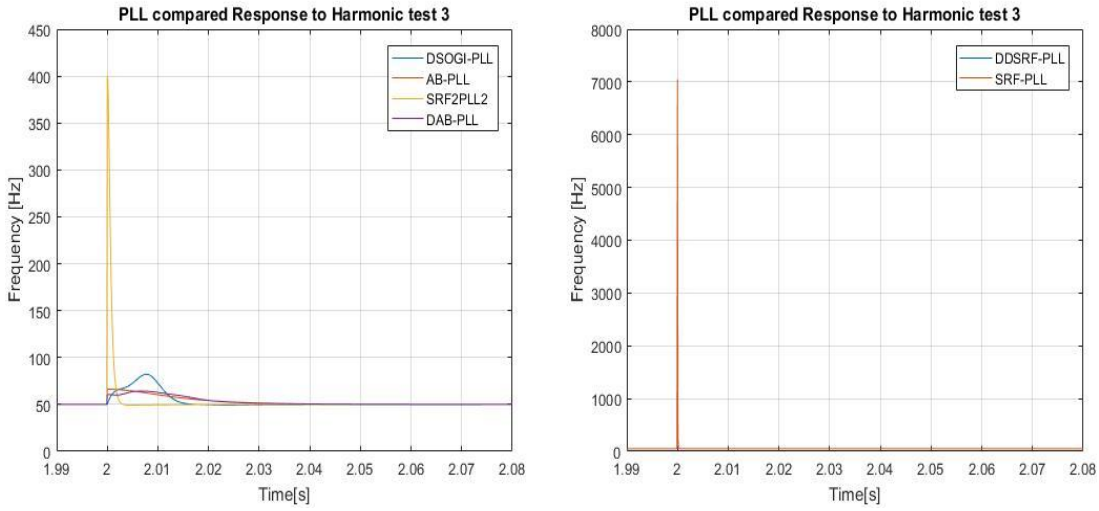


Figure 4.14 Frequency Overhoot during the initial transient phase of the phase jump test

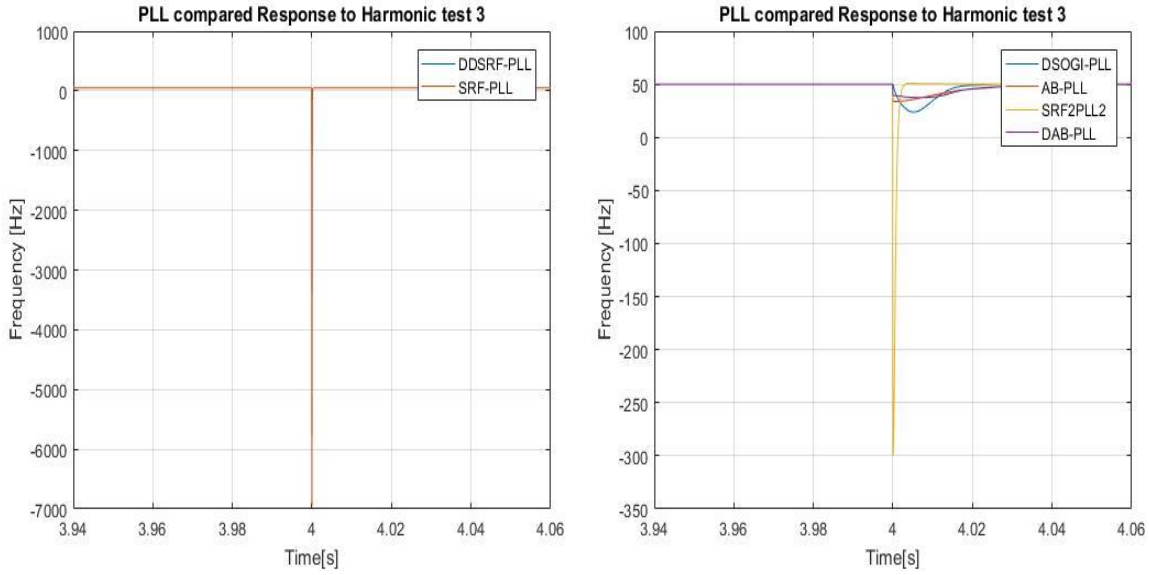


Figure 4.13 Frequency overshoot during the second transient phase of the phase jump test

Since the highest frequency overshoots were seen in the SRF and DDSRF PLL designs, these would probably not be the most adequate choice. In this case, not

having a feedforward improves the dynamic response of the SRF2 over the SRF1 PLL greatly.

4.4. Frequency jumps

Table 4.7 shows the results for both of the frequency jump tests:

		DDSRF-PLL	SRF1-PLL	DSOGI-PLL	AB-PLL	SRF2-PLL	DAB-PLL
2Hz Frequency Jump	Peak Freq Error [Hz]	2.00681417	2.00000267	2.09745546	2.00000029	2.07310766	2.00000041
	Peak Frequency Error [%]	4.01362834	4.00000534	4.19491092	4.00000058	4.14621533	4.00000082
	Peak Phase error [º]	0.02207629	0.01636409	4.40588829	7.06289573	0.28781639	7.69081063
	Ts transient 1 [ms]	<1	<1	134	23	11	23
	Ts transient 2 [ms]	<1	<1	87	41	10	47
	Peak Frequency error 1 [Hz]	2.00681417	2.00000267	2.09745546	2.00000029	2.07310766	2.00000041
	Peak Frequency error 2 [Hz]	2.00000013	6.5346E-09	0.0931735	8.5002E-11	0.07288102	1.481E-10
	Peak Phase error 1 [º]	0.02207629	0.01636409	4.40588829	7.06289573	0.28781639	7.69081063
	Peak Phase error 2 [º]	0.01778688	0.01636394	3.17557251	7.06271511	0.28754137	7.69055708
3Hz Frequency Jump	Peak Freq Error [Hz]	3.0103401	3.00000398	3.12182526	3.00000044	3.10966671	3.00000063
	Peak Frequency Error [%]	6.02068021	6.00000797	6.24365053	6.00000088	6.21933343	6.00000125
	Peak Phase error [º]	0.03347918	0.02454613	6.65968607	10.6283817	0.43173185	11.5802874
	Ts transient 1 [ms]	<1	<1	109	35	<1	43
	Ts transient 2 [ms]	<1	<1	100	45	15	54
	Peak Frequency error 1 [Hz]	3.0103401	3.00000398	3.12182526	3.00000044	3.10966671	3.00000063
	Peak Frequency error 2 [Hz]	3.00000261	3.00000001	3.00003487	3.00000044	3	3.00000063
	Peak Phase error 1 [º]	0.03347918	0.02454613	6.65968607	10.6283817	0.43173185	11.5802874
	Peak Phase error 2 [º]	0.02668057	0.02454605	5.00413048	10.6281085	0.43141405	11.5799014

Table 4.7 Frequency jump test results

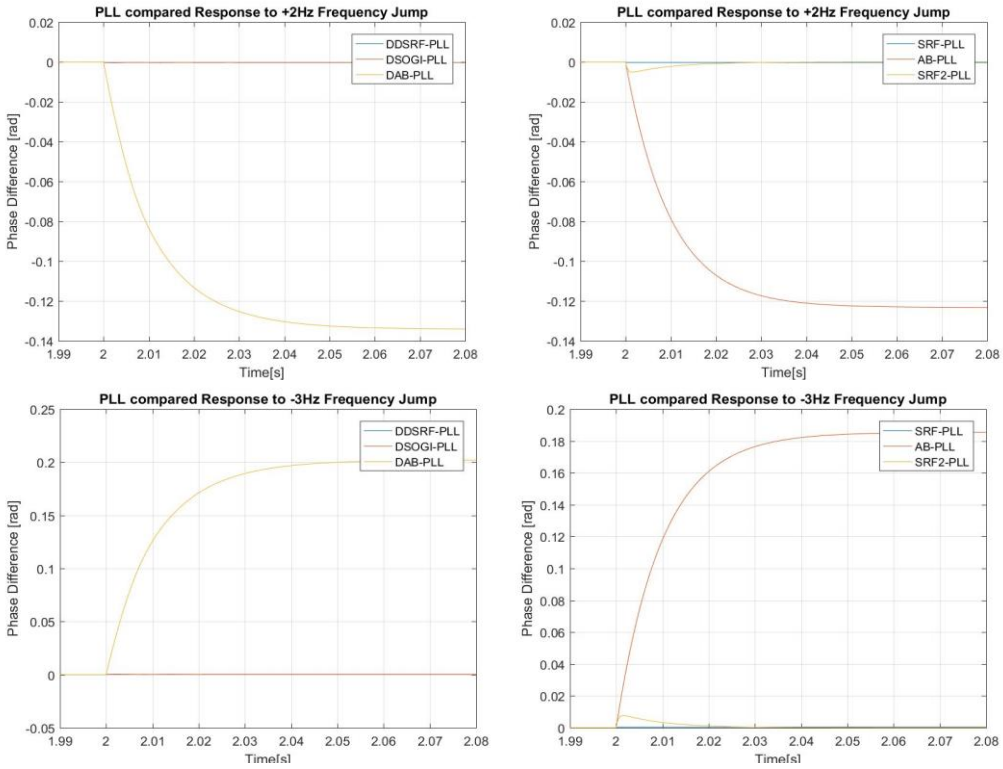


Figure 4.15 Phase difference values for frequency jump tests

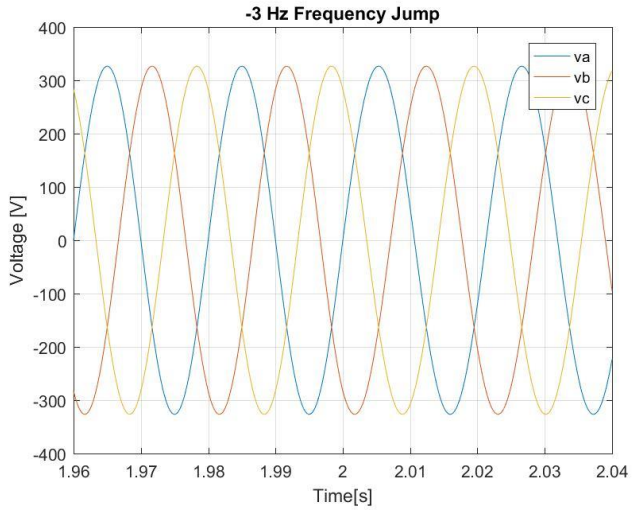


Figure 4.16 -3 Hz Frequency jump test

Variations in the voltage input frequency introduced by these tests do not introduce negative sequence component into the system. Therefore, oscillations in the phase difference values do not occur.

However, both the AB and DAB PLLs experience a fairly big stationary error during the fault. Both these PLLs are the only ones not to feed the Vq voltage value as an input for the PI controller.

As can be seen in fig 4.16, most of the PLLs adapt rapidly to the new frequency. However, the only two PLLs that use a stationary reference frame to determine the phase lose tracking of it during the disturbance.

4.5. Harmonics

The three harmonic tests introduce periodic interferences in the phase output during the fault. The studied PLL designs in this project are incapable of minimising the error as they did under unbalanced voltage sag situations. In this case, the critical part of the PLL that may be able to deal with voltage harmonics is the loop filter.

Table 4.8 summarises the Harmonic test results:

		DDSRF-PLL	SRF1-PLL	DSOGI-PLL	AB-PLL	SRF2-PLL	DAB-PLL
Harmonic Test 1	Peak Freq Error [Hz]	16.4501204	10.3228086	1.08989704	1.09587163	7.3310725	0.97166883
	Peak Frequency Error [%]	32.9002409	20.6456173	2.17979407	2.19174327	14.662145	1.94333765
	Peak Phase error [º]	6.07203265	3.58086549	0.97941202	0.76177123	3.07492632	0.69805228
	Ts transient 2 [ms]	36	1	14	15	2	16
	Peak Frequency error 1 [Hz]	16.4379247	10.3228086	1.08989704	1.09587163	7.3310725	0.97166883
	Peak Frequency error 2 [Hz]	16.4501204	9.55232529	0.97650206	1.02922598	6.88033612	0.90765083
	Peak Phase error 1 [º]	6.07203265	3.58077563	0.97941202	0.76177123	3.07492632	0.69805228
	Peak Phase error 2 [º]	6.06833701	3.58086549	0.60467014	0.48191373	3.0748394	0.42973352
Harmonic Test 2	Peak Freq Error [Hz]	39.7167195	38.8230953	1.34284923	1.79840378	24.2243462	1.62992515
	Peak Frequency Error [%]	79.433439	77.6461906	2.68569846	3.59680756	48.4486924	3.25985029
	Peak Phase error [º]	6.7423761	6.29046836	0.73758066	0.68950888	5.47881031	0.58212219
	Ts transient 2 [ms]	17	1	16	15	1	14
	Peak Frequency error 1 [Hz]	39.7167195	38.8230953	1.34284923	1.79840378	24.2243462	1.62992515
	Peak Frequency error 2 [Hz]	39.7008948	20.9302008	1.17723993	1.74428329	18.5041628	1.53786821
	Peak Phase error 1 [º]	6.7423761	6.29046739	0.73758066	0.68950888	5.47881031	0.58212219
	Peak Phase error 2 [º]	6.73651808	6.29046836	0.51141067	0.48223294	5.1177643	0.45421238
Harmonic Test 3	Peak Freq Error [Hz]	59.0131393	46.1390103	2.01244993	2.38190284	31.448499	2.13584311
	Peak Frequency Error [%]	118.026279	92.2780207	4.02489986	4.76380567	62.896998	4.27168621
	Peak Phase error [º]	11.8593288	8.26111168	1.35207405	1.04419978	6.97341501	0.92664658
	Ts transient 2 [ms]	41	1	16	21	2	22
	Peak Frequency error 1 [Hz]	58.77148	46.1390103	2.01244993	2.38190284	31.448499	2.13584311
	Peak Frequency error 2 [Hz]	59.0131393	20.6295115	1.69135846	2.1942352	18.4085554	1.96924983
	Peak Phase error 1 [º]	11.8593288	8.26100094	1.35207405	1.04419978	6.97341501	0.92664658
	Peak Phase error 2 [º]	11.8575937	8.26111168	1.10006618	0.94558233	6.59526797	0.88104174

Table 4.8 Harmonic test results

Adjusting the filter balancing out the trade-off between a reasonable amount of signal delay and an adequate low-pass filter behaviour where the 50 Hz signal is let through. PLL designs specific for harmonically distorted signals exist. However, due to the difficulties in adjusting and simulating some of those designs, were excluded from the final project.

Upon inspection, one can notice that the settling time after t=2 has not been included in the previous table. The main reason for this is that in the test results, determining this parameter precisely was very difficult and it did not provide particularly useful information.

Even though none of the PLLs was capable of controlling the error during the fault, the values between which this error oscillated were very small in the cases of the DSOGI and the DAB PLLs. Depending on the application, phase estimation errors smaller than 1 degree can be considered acceptable and therefore these choices can withstand small periods of harmonic faults without compromising larger control systems.

Figs 4.17 and 4.18 show the dynamic response of the PLLs to the harmonic 1 test and the voltage input for the test:

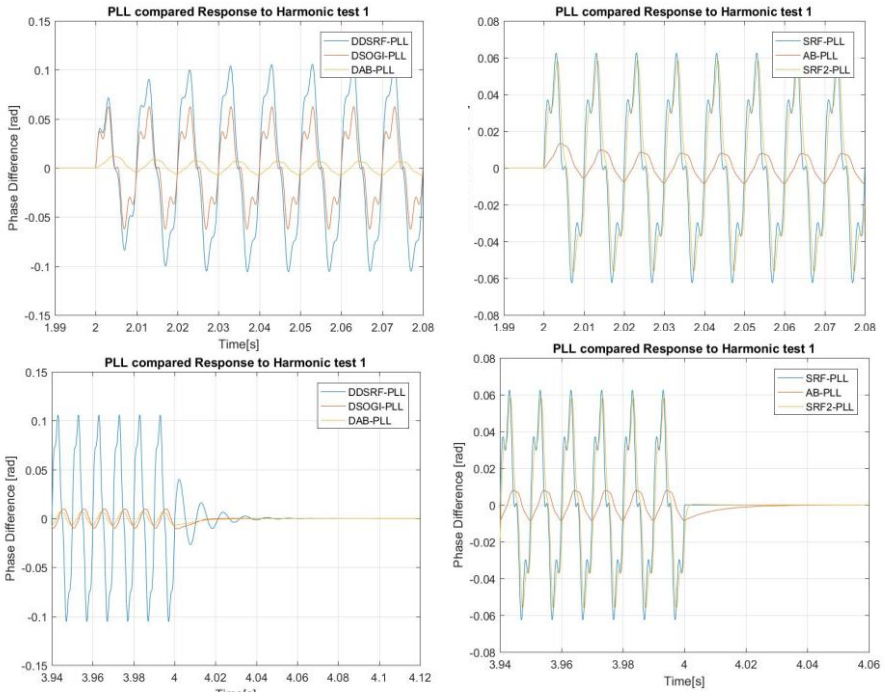


Figure 4.20 Phase difference results for Harmonic test 1

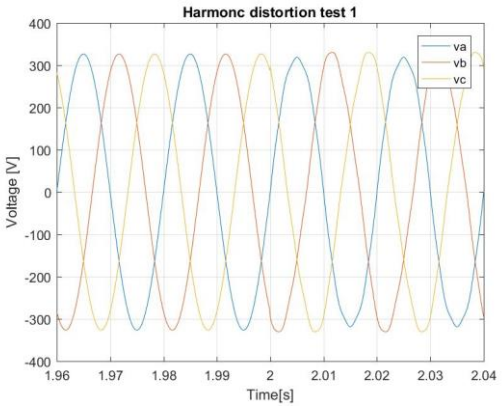


Figure 4.17 harmonic test 1

The harmonic test 2 voltage input can be seen in fig 4.21. Fig 4.22 Shows the dynamic response of the PLLs to the harmonic test 2 in both initial and final transient states:

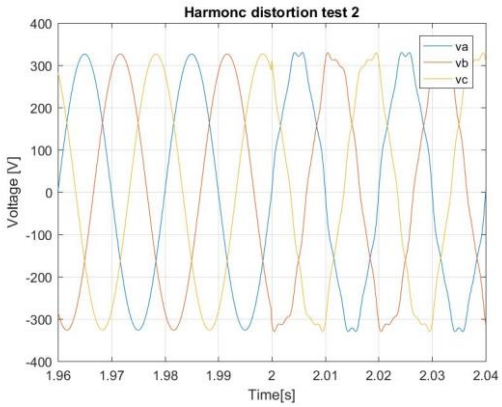


Figure 4.21 Harmonic distortion test 2

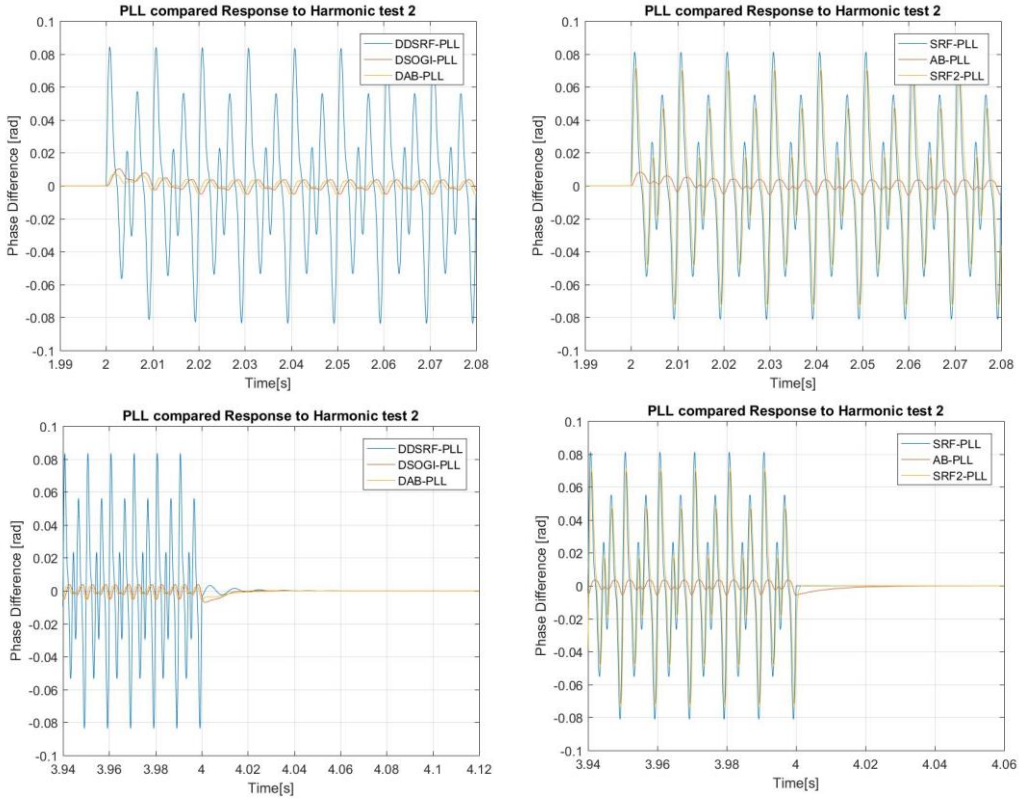


Figure 4.22 Phase difference results for harmonic test 2

Fig 4.23 illustrates the voltage input for the harmonic test 3. Fig 4.24 shows the angle difference values for the harmonic test 3 results.

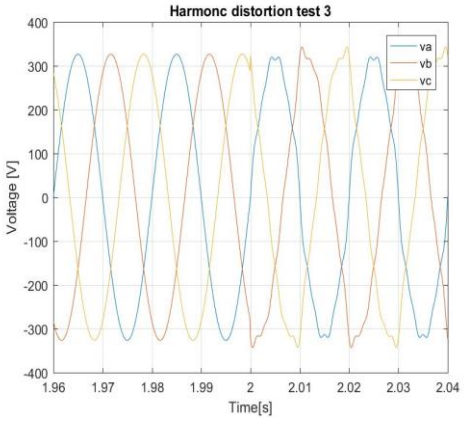


Figure 4.23 Harmonic test 3

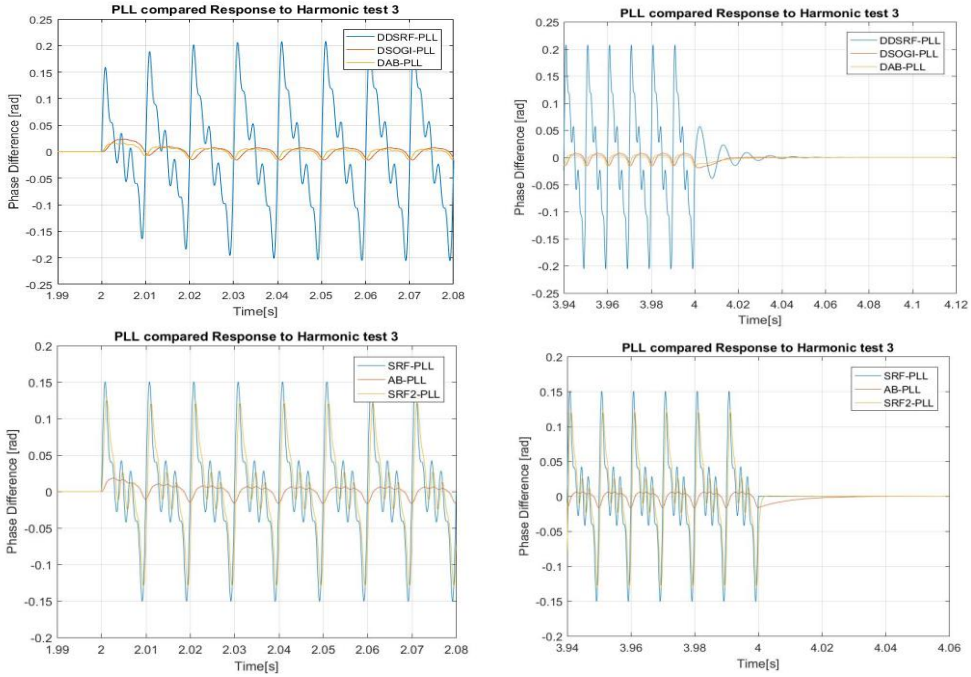


Figure 4.24 Phase difference results for harmonic test 3

The harmonic test 1 only introduces a slight phase imbalance where the shape of the input signal is slightly distorted. The phase error behaves in a similar way in this test as it does in the voltage sag tests. However, in harmonic tests 2 and 3, with the zero-sequence component introduced by the odd multiples of 3 harmonics, the oscillation of this variable is much less comparable to the voltage sag tests. The error falls from the maximum to the minimum with an oscillating component in the way. At the end of the period, the phase difference leaps from -0.15 to 0.15 and the cycle restarts.

Harmonic distortion is not 100% controllable by any of the PLL designs studied in this project. The high frequencies introduced by the harmonics into the signal are considerably present in αß frame making the shape of Vα and Vß impure. This effect is not controllable by the filtering techniques used by the designs which are mostly used to small amplitude differences in Vα and Vß.

The only way if improving the dynamic response of a PLL in a scenario with harmonic distortion is by use of heavy filtering techniques. Some of the excluded PLL designs mentioned in section 2.1.6 are specifically designed to work under highly distorted conditions, but they tend to rely on frequency analysis in discrete time which was the main reason for excluding them.

Upon analysis of the peak phase errors and seeing that the values of these errors are periodic throughout the disturbance, the best performance was found in the DAB, DSOGI and AB PLLs.

Conclusions and Further lines of work

Upon completion of this project, a series of conclusions can be extracted. Firstly, the choice of a PLL not only depends on the input voltage from which the phase will be estimated, it also depends greatly on the type of control loop it will be included in. Therefore, even though this project has successfully introduced 6 PLL designs and has also provided a general description of their behaviour under common voltage faults, each initial PLL choice must then be tailored to fit every specific situation.

Secondly, due to the complexity of some of these designs and the will to focus on studying the general behaviour of the PLLs under standard adjustment, the tuning of the studied designs has not been central to the project. This subject is not a particularly easy one, but taking into account all of the requirements for a PLL within a real system, using robust control techniques to optimise dynamic behaviour of the PLLs could clearly be an interesting next step.

Another important conclusion is that even though this project can provide an insight to the world of the PLLs and serve as an initial choice guide, the theoretical approach to the study can be misleading. These PLLs must be tried under real circuit simulation where they interact with more control loops and see faster and steeper changes in the voltage inputs. Should anyone continue with this project, an obvious continuation would involve testing these PLLs within simulations of real systems like a VSC converter and analysing whether the theoretical response is up to par with the circuit simulation.

Finally, the situations included in the 13 voltage fault tests cover most of the problems encountered in distribution networks. However, there are many more sorts of faults that can be studied. Also, combinations of these tests can also yield interesting results. This study limited the faults to 2 seconds. Should two faults occur in very rapid succession, the system may or may not have time to react. Hence, the study of more complex voltage faults and higher frequency errors is definitely a line of work for the future.

Acknowledgements

I would like to thank all of the people at the CITCEA for their patience and time. Of the countless members of the team who persistently guided me in the search for answers to the many questions posed by this project, I would like to particularly thank Ricard Ferrer, Enric Sanchez and Quim Rebled. Aside from the members of the team, this acknowledgements section could not be complete without mentioning Dr. Eduardo Prieto who not only acted as the tutor of this project and provided pivotal help in its elaboration, but also provided the main motivations behind it.

Thank you for everything!

Appendix A: Budget

In this section, the budget for the project is explained. The budget takes three important aspects into account; office hardware, software and labour costs.

Office hardware

This concept englobes the office equipment needed to conduct the PLL survey and to report the findings of the project as shown in table 0.1:

Concept	Unit. Price	Units	Total
Workstation	1,200 €	1	1,200 €
Total			1,200 €

Table 0.1 Office hardware budget table

The workstation concept includes a high-performance personal computer and the basic peripherals used to interface.

Software and development tools

All of the software licenses and subscriptions to scientific publications are included in this section. Table 0.2 illustrates this:

Concept	Unit. Price	Units	Total
Microsoft Office 2016 student	79 €	1	79 €
Matlab student	500€ (1 year license)	1	500 €
IEEE article subscription	27.85€ (per article)	30	835.50 €
Total			1,414.50 €

Table 0.2 Software and development tool budget table

Labour

The number of hours dedicated to this project are divided research hours, development hours and writing hours (assuming that a junior researcher costs 40€/h). Table 0.3 details the labour budget:

Concept	Unit. Price	Units	Total
Research hours	40€/h	200	8,000 €
Development hours	40€/h	250	10,000 €
Writing hours	40€/h	200	8,000.00 €
Total			26,000.00 €

Table 0.3 Labour concept budget table

Total Budget

Table 0.4 shows the final budget for the whole Project:

Concept	Unit. Price	Units	Total
Workstation	1,200 €	1	1,200 €
Microsoft Office 2016 student	79 €	1	79 €
Matlab student	500€ (1 year license)	1	500 €
IEEE article subscription	27.85€ (per article)	30	835.50 €
Research hours	40€/h	200	8,000 €
Development hours	40€/h	250	10,000 €
Writing hours	40€/h	200	8,000.00 €
Total			28,614.50 €

Table 0.4 Total Budget of the project

The final cost of this project amounts to a total of 28614.5 €.

Appendix B: Environmental Impact

In recent years the environment has seen increased pressure exerted by the production sector and the ever-increasing consumption of goods and commodities on behalf of our society. This is the reason the EU implemented the Strategic Environmental Assessment (SEA Directive) [16] in the year 2001. This directive provides guidelines for the environmental impact assessment of any project.

The aim of this project is to optimise the phase estimation of three-phase voltage signals. The phase estimation is used in bigger control loops which provide stability and optimal operation of power systems like voltage source converters (VSC). Optimising the performance of power systems greatly reduces overall energy losses and can contribute to the production of high exergy power. This is especially important in electrical engineering as an incorrect adjustment of a grid power-injection system could potentially produce unwanted reactive power or voltage disturbances that would propagate throughout the system.

This project consists of an entirely computational simulation of a series of control loops and voltage signals providing numerical results for the study case. This scenario limits the environmental impact of the project to the electricity consumption of the computer and connectivity to the world wide web. Another important aspect is the carbon emissions of the production of computer components which must be compliant with EU regulations. Finally, upon dismantlement of the physical workstation, its components must be disposed of correctly in an electronic waste management site.

Unfortunately, due to the complex structure of the motherboard and other vital components for computational functionality, electronic waste management sites are not capable of recycling a big percentage of the components. This is an issue that must be researched in order to lower the long term environmental impact of computer hardware.

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